

A NEW VARIABLE DIGITAL FILTER DESIGN BASED ON FRACTIONAL DELAY

S. J. Darak, A. P. Vinod
School of Computer Engineering,
Nanyang Technological University,
Nanyang Avenue, Singapore – 639798
 {dara0003.asvinod}@ntu.edu.sg

E. M-K. Lai
School of Engineering & Technology,
Massey University,
Wellington, New Zealand
E.Lai@massey.ac.nz

Abstract— This paper presents a new method for the design of finite impulse response (FIR) filter that provides variable frequency responses. The proposed idea is to replace each unit delay operator in a fixed-coefficient FIR filter with the 2nd order FIR fractional delay (FD) structure and the cutoff frequency, f_c of the filter is changed by changing the FD value. The change in FD results in change in amplitude and length of an impulse response. This in turn changes f_c and transition bandwidth (TBW) of an FIR filter. The mathematical relation between cut-off frequency, TBW and FD value D is derived. The design example shows that the proposed method provides very fine control over f_c .

Index Terms— Variable digital filter, Finite impulse response filter, Farrow structure.

I. INTRODUCTION

In many practical scenarios, it is desirable to change the cut-off frequency of a digital filter in real time with minimal overhead on complexity. Such a filter with variable cut-off frequency, f_c is called as variable digital filter (VDF). They find applications in multi-standard wireless communication receiver (MWCR) systems for channelization involving multiple communication standards, channel equalization, matched filtering and pulse shaping. Finite impulse response (FIR) filters are preferred over infinite impulse response (IIR) filters because FIR filters are linear phase filters with guaranteed stability and low coefficient sensitivity [1]. FIR filters in MWCRs must have low power consumption, low complexity and less reconfiguration time.

There are different methods in the literature to vary the f_c of the digital filter such as programmable filters, coefficient decimation (CD) based VDFs, Farrow structure based VDFs, etc. Programmable filters are the digital filters in which desired cut-off frequency is obtained by updating all the filter coefficients. Several implementation approaches for programmable FIR filters have been proposed in literature [2-5]. The programmable filters are efficient only when f_c needs to be changed occasionally and the order of filter is small. However, for channelization operation where f_c of the filter needs to be changed when the mode of

operation changes, a digital filter which allows the f_c to be controlled by a single parameter, is often desired.

Schuessler and Winkelkemper [6] proposed first transformation approach in which an allpass structure is incorporated in digital filter and f_c is varied by changing the parameters of an allpass structure. Another transformation method to vary f_c of an FIR filter by distorting the frequency axis was proposed in [7]. But the main disadvantages of transformation method is the increase in filter length and the need of special filter structure. The spectral parameter approximation methods using Farrow structure [8] are proposed in [9-11]. In these methods, the overall filter is weighted linear combination of fixed FIR sub-filters; the weights are polynomials of the f_c . This structure has simple updating routine and good filter performance but the overall filter complexity is high.

In [12], the CD methods (CD-I and CD-II) for realizing low complexity reconfigurable FIR filters with fixed coefficients were proposed. The CD-II method allows the passband width of an FIR filter to vary by changing the coefficient decimation factor, M . In CD-II, every M^{th} coefficient of an FIR filter are grouped together discarding in between coefficients to obtain a decimated version of the original frequency response whose passband width and TBW are M times that of the prototype filter [12]. However, the CD-II method [12] is suitable only for designing discretely tunable filter because it is insufficient to provide a low complexity filter realization that has a fine control (increased granularity) over f_c .

In all the VDFs discussed above, f_c is varied over a certain range of frequency by varying single parameter and TBW is either constant [6-11] or greater than the TBW of the original prototype filter (also called as modal filter) [12]. In contrast to the traditional VDFs, the method proposed in this paper is based on replacing each unit delay in an FIR filter with the FIR fractional delay (FD) structure. The change in FD values changes the length and amplitude of the impulse response of an FIR filter. This in turn results in VDFs with tunable f_c whose TBW decreases as the value of FD increases.

The paper is organized as follows. The proposed VDF is presented in Section II. In Section III, mathematical relation

between cut-off frequency, TBW and FD is derived. The design example and implementation results are shown in Section IV and V respectively. Section VI has our conclusion.

II. PROPOSED VARIABLE DIGITAL FILTER

Most of the VDF structures in the literature are based on the basic principle that the frequency specifications of an FIR filter such as f_c and TBW can be changed by modifying its impulse response. The f_c of an FIR filter is equal to the maximum amplitude of an impulse response which in turn depends on the values of the filter coefficients [1]. Also, the TBW of an FIR filter depends on the length of the impulse response which in turn depends on the total number of delays in an FIR filter. The VDF structures in [2-11] are based on modifying the values of the filter coefficients or expressing the filter coefficients in some polynomial forms. However, if the total delay of an FIR filter is changed, the f_c and the TBW changes [12]. In the proposed method, filter coefficients are fixed while the length and the amplitude of an impulse response is modified by replacing each unit delay of the FIR filter with the FIR FD filter structure. By changing the FD, the total number of delays and hence the length and amplitude of an impulse response can be changed. This results in an FIR filter with variable f_c .

The first step in the proposed method is to choose computationally efficient FIR FD filter of appropriate order which can change the FD value in real time. Lagrange interpolation (i.e. Maximally Flat Design) is the most commonly used technique to design an FIR filter approximating a given FD. This is because, Lagrange interpolation has the advantages of smooth magnitude response, easy to calculate coefficients, better response at low frequencies and preferable for applications where a lower order FIR FD filter is needed [13]. Hence, the structure based on Lagrange interpolation is employed in the proposed VDF. Direct form (DF) implementation of Lagrange interpolation needs computationally intensive coefficient update when delay is changed. Hence, DF is not suitable for the proposed VDF where FD must be changed in real time in order to vary f_c . The Farrow structure proposed in [8] as an alternative technique for implementing Lagrange interpolation has the advantages of using fixed-coefficient filters for a given order and real time control of delay [8]. The design of Farrow structure using inverse Vandermonde matrix results in less number of multiplications than the DF structure plus coefficient update, at the cost of adder units [14]. The complexity of the Farrow structure is further reduced in [14] by using the transformation matrix. The structure is called as modified Farrow structure [14].

The order of FIR FD structure, N_d , decides the range of delay produced. For the applications targeted by our method, it is required to change the delay from 1 to 1.05, 1.1, ... up to 2. The mathematical reason for selecting these delay values

is given in Section III. For the given delay range, the suitable value of N_d is 2. The 2nd order modified Farrow structure of Lagrange interpolation [14] is shown in Fig. 1.

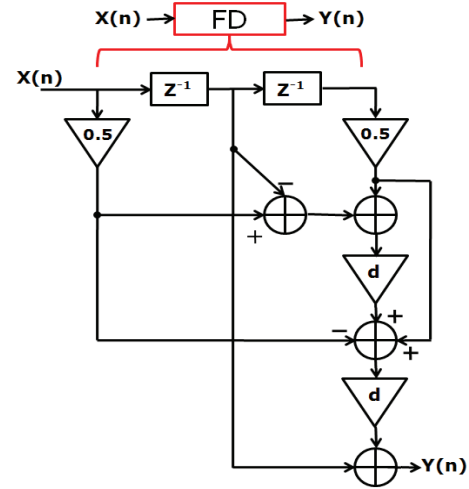


Fig. 1. 2nd Order Modified Farrow structure of Lagrange Interpolation.

The structure in Fig. 1 can be implemented with only two multipliers shown as d because multiplication with 0.5 can be replaced by shift operation. The proposed VDF structure is obtained by replacing each unit delay of a transposed-direct form FIR filter with the modified Farrow structure shown in Fig. 1. Fig. 2 shows the VDF using the proposed method.

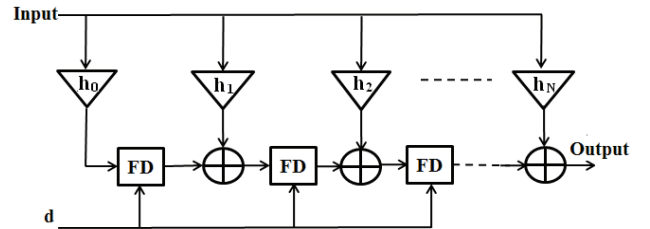


Fig. 2. Proposed VDF structure.

III. RELATION BETWEEN CUT-OFF FREQUENCY, FRACTIONAL DELAY AND TRANSITION BANDWIDTH

In this section, the mathematical relation between the value of FD, D , f_c and TBW is derived for the proposed VDF. First, we represent D as a sum of integer and fractional part.

$$D = \lfloor D \rfloor + d \quad (1)$$

where $\lfloor \cdot \rfloor$ is the floor function and d is the FD ($0 \leq d < 1$). Consider the low pass filter (also called as modal filter) with passband frequency, f_{pass} and stopband frequency, f_{stop} . For

an FIR filter shown in Fig. 2, the length of an impulse response depends on total number of delays, and for FD, $D=1$, with fractional part $d=0$, the length of an impulse response is equal to the length of the modal filter, N_I+1 . As D is changed by varying its fractional part, d , the length of an impulse response changes according to the equation given by,

$$N_D = \lfloor N_I \cdot D \rfloor + 1 \quad (2)$$

where N_D is the length of an impulse response corresponding to D . For an FIR filter with fixed coefficients, the product of TBW_D and length of an impulse response, N_D , is always constant [1].

$$N_D \cdot TBW_D = C \quad (3)$$

where TBW_D is the TBW of an FIR filter corresponding to D . From the specifications of modal filter for $D=1$, constant C is calculated as,

$$C = N_I \cdot TBW_1 \quad (4)$$

From equation (2), it can be observed that as D increases, N_D increases and hence TBW_D decreases according to equation (3). It is well known that the computational complexity of an FIR filter and TBW are inversely proportional to each other. In the proposed method, modal filter can be designed with larger TBW in order to reduce the filter order and hence the complexity; frequency response with sharp TBW can be obtained by increasing D .

Next step is to find the relation between f_c and D . From the impulse response of an FIR filter, f_c is equal to maximum magnitude of an impulse response which occurs at the centre of the impulse response. When D is increased, it is observed that the maximum magnitude of an impulse response and hence f_c decreases. Mathematically, if f_{cD} is the cut-off frequency corresponding to D , then

$$f_{cD} = \frac{f_c}{D} \quad (5)$$

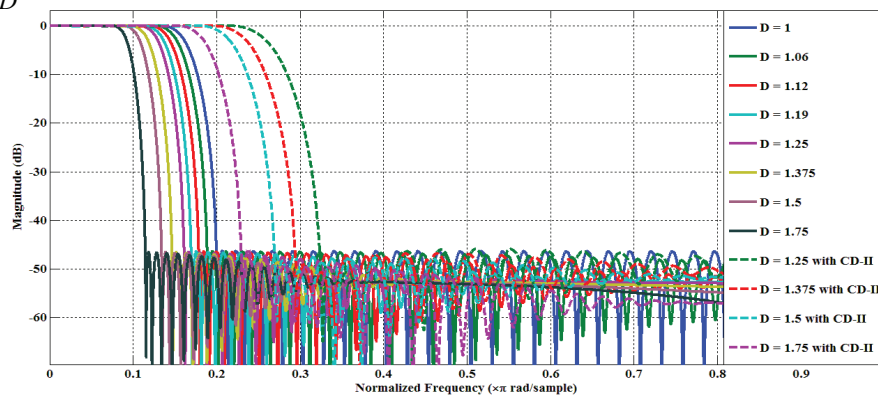


Fig. 3. Variable frequency responses obtained using proposed VDF.

From equation (5), it is noted that the f_{cD} decreases with the increase in D . For integer values of $D > 1$, the filter response consists of multiple subbands. In order to avoid multiband response, D should be less than 2. When D is less than 1, then $f_{cD} > f_c$ and $TBW_D > TBW$. Similar results can be obtained by incorporating CD-II with the proposed VDF as shown in Section IV. Hence, the range of delay for the proposed VDF is selected as $1 \leq D < 2$. Finally, we can obtain f_{pass} and f_{stop} of the modal filter corresponding to D from f_{cD} and TBW_D .

IV. DESIGN EXAMPLE

In this example, a lowpass filter with tunable f_c is designed using our method. The modal filter of order 80 is designed with $f_{pass} = 0.14$ and $f_{stop} = 0.20$. All the frequency edges mentioned here are normalized frequencies with respect to sampling frequency. The TBW of the filter is 0.06 and constant C is 4.86 according to (4). Variable frequency responses of filter obtained using our method for different values of D are shown in Fig. 3 using different colours. Fig. 3 also includes the frequency responses obtained by combining the CD-II method with our method. In our method, delay D can take any value. For the design example considered here, delay D can have 8 different values. Table I shows the f_{pass} and f_{stop} for different values of D . Note that very fine control over f_c is achieved using our method.

The complexity of an FIR filter is dominated by the number of coefficient multiplications. Hence, the complexity of the filter realized using our method is expressed in terms of number of real multiplications required per output cycle. Using conventional implementation of modified Farrow structure, the number of real multiplications per output cycle required in our method would be $2.5 \times N_I$ ($2N_I$ considering 2 multiplications for each modified Farrow structure, and $0.5N_I$ multiplications for the symmetric half coefficients) where N_I is the order of the modal filter. However, by selecting D values as given in Table I, the number of real

multiplications is reduced to $0.5 \times N_1$ by realizing multiplications with d using hardwired shifts and additions. As $TBW_D \leq TBW_1$, the complexity of the filter can be reduced by designing the modal filter with larger TBW and hence smaller order, N_1 . For example, the fixed-coefficient FIR filter with $TBW=0.034$ will require 0.5×164 real multiplications as compared to 0.5×81 in our method. However, for the cases where D can have any value, number of multiplications in our method is 0.5×203 .

TABLE I. SPECIFICATIONS OF f_{pass} AND f_{stop} FOR DIFFERENT D

D	f_{cD}	TBW_D	f_{pass}	f_{stop}	Our method + CD-II [12]	
					f_{pass}	f_{stop}
1	0.17	0.06	0.14	0.20	NA	NA
1.0625	0.16	0.0565	0.132	0.188	NA	NA
1.125	0.152	0.0535	0.125	0.178	NA	NA
1.1875	0.143	0.0504	0.118	0.168	NA	NA
1.25	0.136	0.0480	0.112	0.16	NA	NA
1.375	0.124	0.0439	0.100	0.146	0.2	0.292
1.5	0.113	0.0400	0.093	0.133	0.186	0.266
1.75	0.097	0.0344	0.08	0.114	0.16	0.228

V. IMPLEMENTATION RESULTS

We have implemented the design example discussed in Section IV on Xilinx Virtex 2v3000ff1152-4 FPGA associated with the dual DSP-FPGA Signal master kit provided by Lyrtech [15]. Our objective is to test the functionality of the architecture by changing the f_c in real time. The total equivalent gate count and total slices required for the proposed architecture are 430849 and 13301 respectively. The static power consumption is 81 mW. In programmable filters [2-5], filter coefficients are not fixed and memory is required to store the filter coefficients. In the proposed architecture, filter coefficients are fixed and hence complexity can be further reduced by replacing the multiplication operation with hardwired shifts and additions. Also, memory is not required for the proposed method.

VI. CONCLUSION

A new method for the design of an FIR filter with variable frequency responses is proposed. In the proposed method, filter coefficients are fixed while each delay of an FIR filter is replaced with 2nd order FIR fractional delay (FD) which can change delay in real time. The change in FD results in corresponding change in the length and amplitude of an impulse response. This in turn results in variable digital filter (VDF) whose cut-off frequency, f_c , and transition bandwidth, TBW, decreases as the value of FD, D , increases. The mathematical relation between FD value D , f_c and TBW is derived and implementation results are discussed. The design example shows that our method

provides very fine control over f_c . The Farrow structure of order 2 has flat magnitude response only up to frequency 0.2. As per our knowledge, computationally efficient lower order structure which provides the variable FD with flat magnitude response for the frequency greater than 0.2 is not available in the literature. Hence, in order to obtain the f_c greater than 0.2 and to reduce the complexity when D can have any value, the future work will focus on combining the proposed method with an appropriate method.

VII. REFERENCES

- [1] S.K. Mitra, *Digital Signal Processing: A Computer-Based Approach*, Singapore: McGraw-Hill, 1998.
- [2] T. Solla and O. Vainio, "Comparison of programmable fir filter architectures for low power," in *Proc. of 28th European Solid-State Circuits Conference*, pp. 759-762, Firenze, Italy, Sep. 2002.
- [3] T. Solla, R. Mäkelä, M. Liljeroos, and O. Vainio, "Application-specific filter processor for flexible receivers," in *Proc. of 19th NORCHIP Conference*, pp. 53-58, Kista, Sweden, Nov. 2001.
- [4] K. H. Chen and T. D. Chiueh, "A low-power digit-based reconfigurable FIR filter," *IEEE Trans on Circuits and Systems-II*, vol. 53, no. 8, pp.617-621, Aug. 2006.
- [5] P. Tummeltshammer, J. C. Hoe and M. Puschel, "Multiplexed Multiple Constant Multiplication," *IEEE Trans on Computer Aided Design of Integrated Circuits*, vol. 26, no. 9, pp. 1551-1563, Sep. 2007.
- [6] W. Schiessler and W. Winkelnkemper, "Variable digital filters," *AEU*, vol. 24, pp. 524-525, 1970. Reprinted in *Digital Signal Processing*, L. R. Rabiner and C. M. Rader, Eds. New York: IEEE Press, 1972.
- [7] A. V. Oppenheim, W. F. G. Mechlenbräuker, and R. M. Mersereau, "Variable cutoff linear phase digital filters," *IEEE Trans. Circuits Syst.*, vol. 23, pp. 199-203, Apr. 1976.
- [8] C. W. Farrow, "A continuously variable digital delay element," in *Proc. IEEE ISCAS'88*, Espoo, Finland, Jun. 1988, pp. 2641-2645.
- [9] S. C. Chan, C. K. S. Pun, and K. L. Ho, "A new method for designing FIR filters with variable characteristics," *IEEE Signal Process. Lett.*, vol. 11, pp. 274-277, Feb. 2004.
- [10] T. B. Deng, "Weighted least-squares method for designing arbitrarily variable 1-D FIR digital filters," *Signal Process. (Elsevier)*, vol. 4, pp. 597-613, Apr. 2000.
- [11] P. Löwenborg and H. Johansson, "Minimax design of adjustable-bandwidth linear-phase FIR filters," *IEEE Trans. Circuits Syst. I*, vol. 53, pp. 431-439, Feb. 2006.
- [12] R. Mahesh and A. P. Vinod, "Coefficient decimation approach for realizing reconfigurable finite impulse response filters," *Proceedings of IEEE international symposium on circuits and systems*, seattle USA, May 2008.
- [13] T. Laakso, V. Valimäki, M. Karjalainen, and U. Laine, "Splitting the unit delay," *IEEE Signal Processing Mag.*, vol. 13, pp. 30-60, 1996.
- [14] V. Valimäki, "A new filter implementation strategy for Lagrange interpolation," *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 361-364, 1995.
- [15] http://www.lyrtech.com/DSPdevelopment/dsp_fpga/signalmas ter_quad_cpci.php.