A Reconfigurable Multi-standard Channelizer using QMF trees for Software Radio Receivers

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***Abstract*—The flexibility of a software-defined radio (SDR) depends on its capability to operate in multi-standard wireless communication environments. The most computationally intensive part of wideband receivers is the channelizer, which extracts multiple narrowband signals from adjacent frequency bands. In an SDR receiver, the compatibility of the channnelizer with different communication standards is guaranteed by its reconfigurability. This paper presents an efficient channelizer that has a reconfigurable architecture based on quadrature mirror filter bank (QMF) trees. We show that the channelizer can be efficiently implemented using common subexpression based filter structures. An example of dual-mode Global System for Mobile Communication (GSM)/Personal Digital Cellular (PDC) channelizer is discussed to illustrate the proposed design methodology.**

Keywords-Software radio, quadrature mirror filter bank, dual-mode channelizer, common subexpressions, canonic-signed digit.

I. INTRODUCTION

SDR migrates the traditional hard-wired radio platforms to flexible software definable platforms that can support multiple air interface standards [1], [2]. A first order estimate of the resources required to implement the wideband receiver of a software radio shows that the intermediate frequency (IF) processing block to be the most computationally intensive part since it operates at the highest sampling rate [1]. A reconfigurable IF processing architecture for the extraction of individual channels can significantly reduce the cost and complexity of cellular base stations. Efficient implementations of channelizer have been proposed using Discrete Fourier Transform (DFT) filter bank [3], [4]. The basic principle of the DFT filter bank channelizer is to simultaneously extract a number of equally spaced channels using a uniform filter bank derived from the modulation of a given prototype filter as shown in Fig. 1. The filter bank channelizer extracts every channel between $[(-F_S/2),(F_S/2)]$, where F_S is the sampling frequency of the wide-band ADC. The complexity of a filter bank channelizer is independent of the number of received channels. However, DFT filter banks cannot perform channelization for channels with different bandwidth. This is so since DFT filter banks are modulated filter banks with equal bandwidth of all bandpass filters. Therefore, it can only support a given air interface standard. Hence each cellular standard would require a distinct channelizer to extract its channels. Multi-mode receivers discussed in the literature [5], [6] employ distinct filter bank channelizers for each cellular communication mode. This paper presents the implementation of a reconfigurable channelizer using QMF trees and its efficient implementation employing common subexpressions. The paper is organized as follows. Section II presents the reconfigurable architecture of the proposed channelizer. We discuss a hardware efficient implementation of channel filters in Section III. In section IV, we illustrate the realization of a dual-mode GSM/PDC channelizer receiver using a design example. Section V provides our conclusions.

II. TREE STRUCTURED QMF BANK CHANNELIZER

It is well known that tree-structured QMF banks are employed in the implementation of discrete wavelet transform [7]. Basically, the QMF tree decomposes the input signal into several frequency subbands. We employ the tree-structured QMF bank shown in Fig. 2 to perform channel extraction from a wideband received signal. The input bandwidth of the IF signal from the radio frequency (RF) module will cover several channels of different communications standards. The QMF analysis banks split the signal into several subbands down the tree. Thus, channel extraction in this multistage channelizer is performed at a stage whose subband corresponds to the channel spacing of the current mode of operation.

In conventional multi-mode receivers, many individual channelizers are required to support different communications standards in one single cellular base station. Thus, reconfigurability of such receivers is constrained to switching the operation among distinct channelizers based on the current mode. This is an inefficient approach due to its increased hardware complexity and power consumption. *We define reconfigurability as the ability to reprogram the same channelizer to work with different standards.* The proposed multi-standard channelizer offers reconfigurability in two levels, namely, architecture level and filter level.

A. Architecture Reconfigurability

The reconfigurability of the channelizer architecture can be illustrated using the tree-structured QMF bank shown in Fig. 2. For simplicity, a dual-mode operation is considered. Let the sampling frequency of the input signal be F_s, and f_{cs_1} and f_{cs_2} represent the channel spacing of modes 1 and 2

respectively, where $f_{cs_1} = n f_{cs_2}$ and n is an even integer. Employing the proposed architecture, the channels of mode 1 can be extracted at the output of stage, s_1, and that of mode 2 at the output of stage, s_2, in respective mode of operation, where s_1 and s_2 are give by the expressions:

$$2^{s_1} = [F_s/2]/f_{cs_1} \text{ and } 2^{s_2} = [F_s/2]/f_{cs_2} \quad (1)$$

Hence the same set of analysis filter banks are used to extract channels in both modes. Reconfigurability is achieved by selecting the channels from the desired stage for a specific mode. Thus, the same QMF tree can be reprogrammed to adapt to a new communications standard by choosing the appropriate subband decomposition level down the tree.

B. Filter Reconfigurability

The low-pass filter, H_0, employed in all stages will have identical coefficients since the signal is decimated by two in each stage. Given a peak passband ripple specification δ_1 and a peak stopband ripple specification δ_2, the minimum order linear-phase equiripple FIR filter that meets these specifications [8] has a length

$$P = [2\log_{10}(1/10\delta_1\delta_2)]/3\Delta f \quad (2)$$

where $\Delta f = (\text{stopband edge-passband edge})/(2\times\pi)$. Let δ_2' and δ_2'' be the peak stopband ripple specifications of two communications standards in a dual-mode channelizer such that $\delta_2'' > \delta_1'$. Assuming identical δ_1 and Δf for both standards, we obtain respective low-pass filters, H_0' and H_0'', with lengths P_1 and P_2 such that $P_2 > P_1$. Since the QMF bank decomposes the input signal at quadrature frequency, 0.5π, H_0' can be directly obtained from H_0'' by truncating the latter to length, P_1. In other words, the symmetric P_1 coefficients of H_0'' are same that of H_0'. In a multi-standard platform, we fix the length of H_0 based on the blocker specifications of the communications standard that requires the most attenuation. We designate this filter, which has the highest order as the 'parent filter'. When the channelizer switches from the mode that requires maximum stopband attenuation to another mode, the software truncates the parent filter to a length corresponding to the attenuation requirement of the new standard. It may be noted that the parent filter itself can be employed in the new mode, as it will offer attenuation more than the specification. However, the reduced filter order after truncation will result in hardware reduction and the desired attenuation is still maintained. Since the coefficients of the parent filter, H_0, form the superset of all other low-pass filters obtained by truncating the former, we can use a fixed-coefficient structure to implement the parent filter. Employing the same parent filter structure, the filter length can be reprogrammed to work with the new mode by reconfiguring the signal flow to delay taps corresponding to the filter length of the mode. In other words, filter structure and coefficients are same and only the number of taps need to be changed. In the following section, we exploit the fixed-coefficient property of the parent filter to realize hardware efficient channel filter structures.

III. LOW-COMPLEXITY CHANNEL FILTER STRUCTURES

A. Analysis Filter bank Realization

Since the high-pass filter, H_1, is the inverse of the low-pass filter, H_0, in a QMF bank, the former can be obtained from the latter using the relation [7], $h_1(n) = (-1)^n h_0(n)$. The output of the low-pass filter of length N is given by:

$$y_0(n) = h(0)x(n) + h(1)x(n-1) + \ldots\ldots + h(n)x(n-N) \quad (3)$$

Using the inverse relation, the output of the high-pass filter is:

$$y_1(n) = h(0)x(n) - h(1)x(n-1) + \ldots\ldots + h(n)x(n-N) \quad (4)$$

Therefore, $y_1(n)$ can be obtained from $y_0(n)$ by keeping the even terms unchanged and negating the odd terms as given by (3) and (4). The filter structure shown in Fig. 3 efficiently extracts the low and high frequency subbands from the input signal by using the same set of coefficients of the prototype low-pass filter. Hence no separate high-pass filters are required to extract the channels and the entire channelizer is built based on the prototype low-pass parent filter, H_0. Therefore, our focus is on the hardware efficient implementation of the parent filter.

B. Parent Filter Structures using Common Subexpressions

It has been shown that using common subexpression elimination (CSE) to exploit redundancy across the canonic signed digit (CSD) coefficients results in filters with minimum number of adders [8]. The CSE method eliminates redundant computations in multiplier blocks by employing the most common subexpressions among the CSD coefficients. We propose to implement the channel filters using CSE method and it can be shown that the resulting hardware efficient filter structure has high degree of reconfigurability. The following example of a dual-mode channelizer illustrates our approach. For the purpose of illustration, we choose filters with fewer numbers of taps and it must be noted that higher order filters are required in the practical scenario.

We consider a parent filter of length, $N_1 = 9$, for mode 1 corresponding to the communications standard that requires maximum stopband attenuation. Assume the length of the filter for mode 2 be $N_2 = 5$, which is obtained by truncating the parent filter. The CSD form of the parent filter is shown in Fig. 4. Common subexpressions 101 and 10-1 indicated by circles are given by $x_2 = x_1 + x_1 >> 2$ and $x_3 = x_1 - x_1 >> 2$ where >> represents the 'shift right' operation and x_1 represents the input signal. The output of the parent filter is obtained as:

$$y = x_2 >> 7 + x_3 >> 12 + x_1[-1] >> 4 - x_3[-1] >> 8 +$$
$$x_2[-1] >> 14 - x_3[-2] >> 4 + x_2[-2] >> 10 - x_1[-2] >> 15 +$$
$$x_2[-3] >> 2 + x_3[-3] >> 7 + x_1[-4] >> 1 + x_2[-5] >> 2 +$$
$$x_3[-5] >> 7 - x_3[-6] >> 4 + x_2[-6] >> 10 - x_1[-6] >> 15 +$$

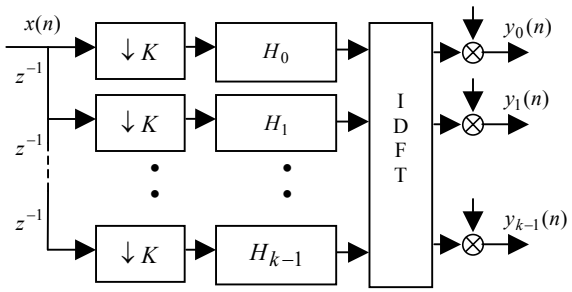

Figure 1. Classical DFT filter bank channelizer

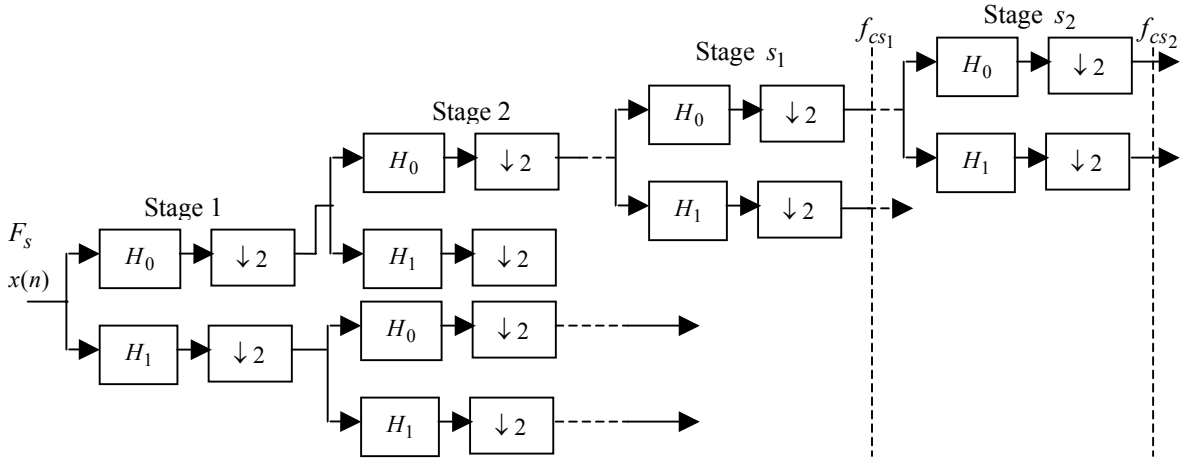

Figure 2. Multimode channelizer based on tree structured QMF bank

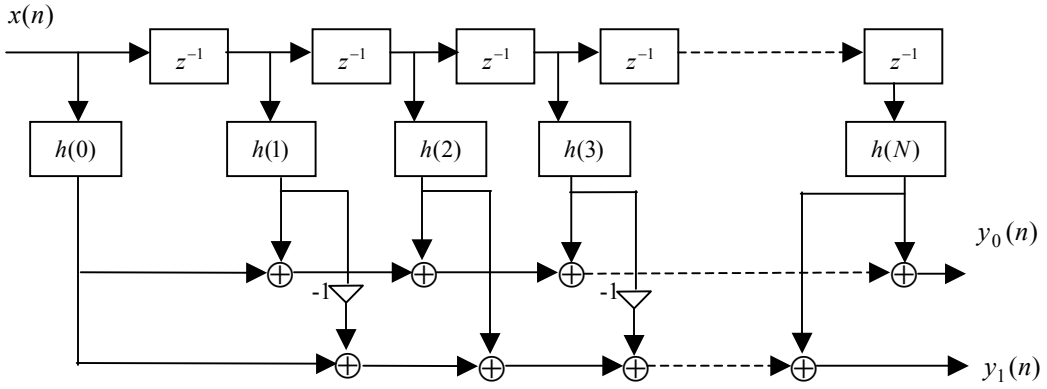

Figure 3. Filter Structure for obtaining the subbands $y_0(n)$ and $y_1(n)$

	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16
h(0)							1		1			1		-1		
h(1)				1				-1		1				1		1
h(2)				-1		1				1		1			-1	
h(3)		1		1			1		-1							
h(4)	1															
h(5)		1		1			1		-1							
h(6)				-1		1				1		1			-1	
h(7)				1				-1		1				1		1
h(8)							1		1			1		-1		

Figure 4. CSD form of the QMF prototype low-pass filter

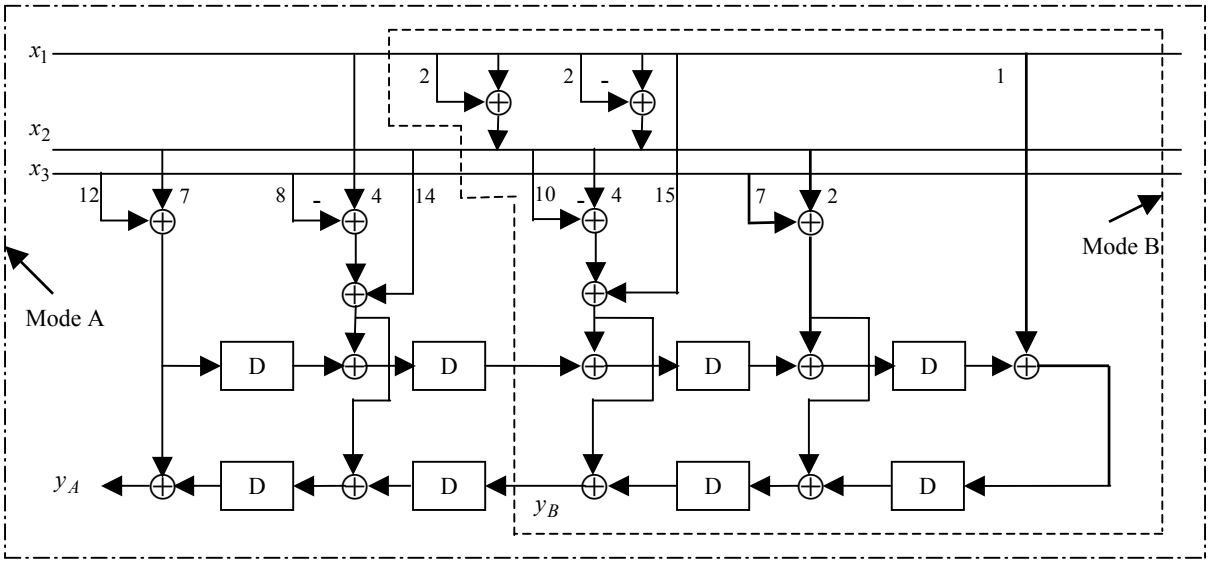

Figure 5. Proposed reconfigurable filter structure for dual mode channelizer

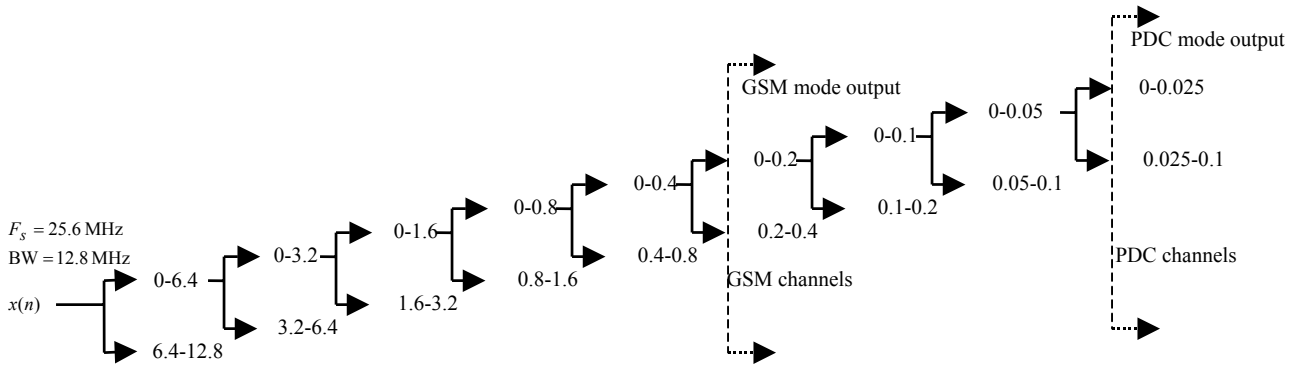

Figure 6. Tree structure for the dual-mode GSM/PDC channelizer in design example.
(Channel spacing in MHz)

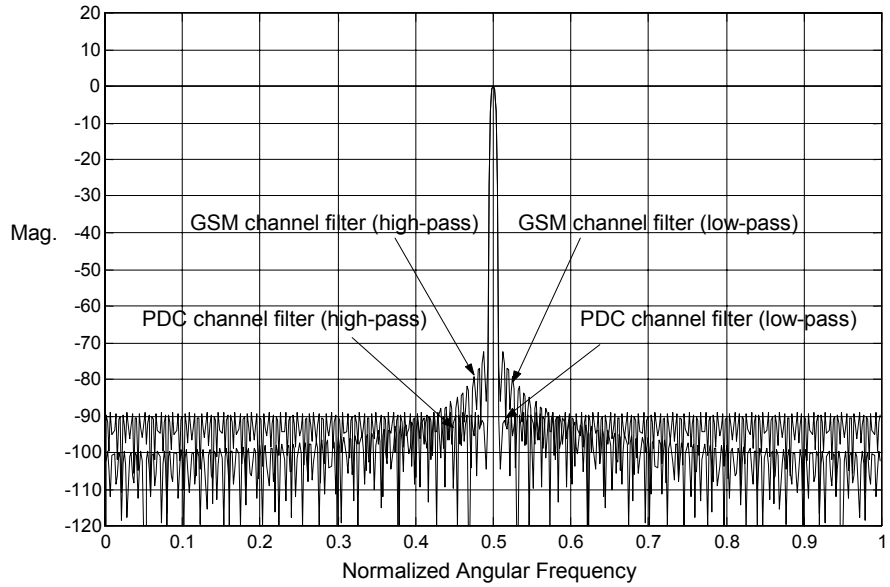

Figure 7. Magnitude responses of the GSM and PDC channel filters in design example

$$x_1[-7] >> 4 - x_3[-7] >> 8 + x_2[-7] >> 14 + x_2[-8] >> 7 + x_3[-8] >> 12 \quad (5)$$

where [-*k*] represents the delay operation. The resulting filter can be implemented using the transposed direct form FIR filter structure as shown in Fig. 5. It can be noted that only sixteen adders are required to implement the parent filter indicated as 'mode A' in Fig. 5. Conventional CSD implementation would require twenty-two adders and hence the CSE method results in reduction rate of 27% when compared to the former. From the filter structure, it can also be seen that the adder requirement is reduced to ten corresponding to filter length, $N_2 = 5,$ when the channelizer operates in 'mode B'. Furthermore, the same filter structure is used for both modes, except that the signal flow is reconfigured to the delay tap of the respective mode of operation. Thus the filter structure remains unaltered since the coefficients are fixed and this will significantly reduce the routing complexity.

IV. DESIGN EXAMPLE

In this section, we show the implementation of a tree structured QMF bank channelizer for a dual-mode GSM/PDC software radio receiver. PDC is a TDMA based system with an infrastructure that is very similar to GSM and is widely deployed in Japan. The architecture of the channelizer is shown in Fig. 6. The input bandwidth of IF signal from RF module will cover several channels of GSM and PDC. The channel spacing of GSM and PDC are 200 kHz and 25 kHz respectively. The sampling rate for both GSM and PDC is chosen as 25.6 MHz and a bandwidth of 12.8 MHz is considered. The tree structured QMF analysis banks perform decomposition of input signal into subbands in multiple stages. For simplicity, only a part of the subband decomposition along the tree structure has been shown in Fig. 6. However, in the actual implementation, the entire frequency band of the input signal will be decomposed using the QMF tree to extract every channel. When the channelizer operates in GSM mode, the output signal is extracted from the sixth stage of the tree whose bandwidth is 200 kHz. To interface directly to the baseband processing block, the sampling rate of the extracted signal must be a small integer multiple of the baud rate [3]. Hence the extracted GSM signal is fed to the baseband processing block after sample rate conversion (SRC). In PDC mode, signal is extracted from the last stage whose bandwidth is 25 kHz and is fed to the baseband processing block after SRC. The channel filters need to attenuate blockers that can be potentially 76 dB stronger than the wanted signal in GSM mode where as the attenuation requirement is 90 dB in PDC mode as in the specifications [10]. Using (2), respective filter lengths are obtained as $P_1 = 1100,$ and $P_2 = 1400.$ We fix the PDC mode filter of length 1400 as the parent filter. The filter of length 1100 for GSM mode is directly obtained from the parent filter by truncation. The magnitude responses of the analysis filter bank are shown in Fig. 7. It may be noted that the passband and transition band responses of both filters are identical and the GSM filter obtained by truncating the PDC filter maintains stop-band attenuation of 76 dB as required. The reconfigurable filters implemented using CSE results in a minimum adder structure offering a reduction of 35% when compared to conventional CSD implementation.

V. CONCLUSIONS

A reconfigurable tree structured QMF bank channelizer for multi-standard software radio receiver is presented in this paper. While in conventional multi-mode receivers, each cellular standard would require a distinct channelizer, the proposed architecture needs only one channelizer due to its high degree of reconfigurability. The key feature of the channelizer presented is its hardware reconfigurability achieved with minimum routing complexity. In the proposed multistage channelizer, reconfigurability in architecture level is achieved by extracting the signal from the tree-stage corresponding to the desired channel spacing. The entire channelizer is built based on a fixed-coefficient prototype low-pass parent filter. Thus reprogramming the filter for a different communication standard refers to truncating the parent filter length so as to satisfy respective specification. Since the filter structure as well as coefficients remains unchanged, considerable hardware optimization is achieved. Efficient implementation of channel filters using common subexpressions is proposed. An example dual-mode GSM/PDC channelizer is also discussed to illustrate the proposed design methodology. The proposed architecture can be easily reconfigured for other wireless communications standards.

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