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A Low Complexity Reconfigurable Non-uniform Filter Bank for Channelization in Multi-standard Wireless Communication Receivers

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Abstract In a typical multi-standard wireless communication receiver, the channelizer must have the capability of extracting multiple channels (frequency bands) of distinct bandwidths corresponding to different communication standards. The channelizer operates at the highest sampling rate in the digital front end of receiver and hence power efficient low complex architecture is required for cost-effective implementation of channelizer. Reconfigurability is another key requirement in the channelizer to support different communication standards. In this paper, we propose a low complexity reconfigurable filter bank (FB) channelizer based on coefficient decimation, interpolation and frequency masking techniques. The proposed FB architecture is capable of extracting channels of distinct (non-uniform) bandwidths from the wideband input signal. Design example shows that the proposed FB offers multiplier complexity reduction of 83% over Per-Channel (PC) approach and 60% over Modulated Perfect Reconstruction FB. The proposed FB when designed as a uniform FB (subbands of equal bandwidths), offers a complexity reduction of 20% over Discrete Fourier Transform FB (DFTFB) and 57% over Goertzel Filter Bank. Furthermore, the proposed FB has an added advantage of dynamic reconfigurability over these FBs. The proposed FB is implemented on Xilinx Virtex 2v3000ff1152-4 FPGA with 16 bit precision. The PC approach and DFTFB are also implemented on the same FPGA with 14 bit precision. The implementation results shows an average slice reduction of 29.14% and power reduction of 46.84% over PC approach, 14.39% and 2.67% over DFTFB.

Keywords Multi-standard wireless communication receivers · Channelization · Coefficient decimation · Reconfigurability

1 Introduction

The software defined radio (SDR) based multi-standard wireless communication receivers (MWCR) enable different air-interfaces to be implemented on a single generic hardware platform by replacing conventional analog signal processing with the digital signal processing. The most computationally intensive and power consuming block in the digital front end of a MWCR is the channelizer, which operates at the highest sampling rate [1]. Channelization involves digital down conversion, channel filtering and sample rate conversion. Basically, the channelizer is employed to extract individual radio channels (frequency bands) from the wideband input signal for follow-on baseband processing [2]. In MWCRs, channelization is usually done using a digital filter bank (FB). The FB must be dynamically reconfigurable which means that the same FB can be reconfigured for a new communication standard with minimum overhead, instead of employing separate FBs for each standard. Such a dynamically reconfigurable FB must be capable of extracting non-uniform bandwidth (BW) channels corresponding to different communication

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standards from wideband input signals. Moreover, the FB should meet the stringent specifications of minimum area, delay and power for efficient hardware implementation.

In this paper, we present a reconfigurable FB channelizer for MWCRs based on interpolation, coefficient decimation (CD) and frequency masking techniques. Reconfigurability is achieved by suitably changing decimation value, which will result in variable BW subbands. The number of subbands in proposed FB is fixed and BW of subbands is varied using appropriate decimation factors.

The paper is organized as follows. In section 2, a review of FBs and CD technique [3] is presented. In section 3, the design of the proposed FB is explained. Section 4 describes the architecture of proposed FB. In Section 5, functionality test of proposed FB is discussed and section 6 presents multiplication complexity comparison with other FBs. In Section 7, implementation results are presented. Section 8 has our conclusion.

2 Literature Review

In this section, we review existing FBs in the literature and the CD technique proposed in [3]. We will also discuss suitability of FBs for uniform and non-uniform channelization in MWCRs.

2.1 Review of Filter Banks

The per-channel (PC) approach [4] is a Velcro approach in which each distinct channel is extracted using a dedicated filter. The PC approach can support uniform as well as non-uniform channelization. The complexity of the PC approach increases with the number of received channels. Also, PC approach requires separate channelizer for each standard along with digital down conversion [4]. Because of these shortcomings, PC approach is not a hardware efficient solution.

Discrete Fourier transform filter bank (DFTFB) is widely employed when multiple channels of the same communication standard need to be extracted. DFTFB is a modulated FB consists of a single low pass filter followed by DFT operation [2, 4, 5]. The limitations of DFTFBs are, 1) All the channels are of uniform BW i.e. DFTFBs cannot extract channels with distinct BWs simultaneously, and 2) Fixed channel stacking. Therefore, distinct DFTFBs and sample rate converters are required for each standard supported by MWCRs. Hence, when DFTFB-based channelizer is employed, the complexity of MWCRs increases linearly with number of operating standards. A modulated FB based on a combination of polyphase FB and DFT modules has been proposed in [6]. This hybrid FB is computationally efficient when compared to conventional DFTFBs. But the FB in [6] is incapable of extracting non-uniform channels. DFTFB and its modifications are expensive when channels of multiple standards need to be extracted.

A Goertzel filter bank (GFB) [4] based on Goertzel algorithm is a modulated FB provides solution to fixed channel stacking problems. But there is no consideration on implementation complexities of GFB and it cannot extract channels of different BWs [4]. In multi-standard environment, the polyphase implementation of prototype filter makes reconfiguration tasks more tedious and expensive as it invokes updation of polyphase branches and the coefficients. Also, the GFB may encounter stability problem while reformulating the DFT because infinite impulse response filters are used in the implementation of DFT based on modified Goertzel algorithm.

A channelizer based on modulated perfect reconstruction filter bank (MPRFB), which can extract channels of non-uniform BWs, is proposed in [7]. The MPRFB consists of an analysis section and a synthesis section. BWs of channels extracted by synthesis section are integer multiples of BW of the subband channels extracted by analysis section which limits the flexibility of the MPRFB in a multi-standard environment. Hence, the MPRFB fails to extract channels of communication standards whose BWs are not related by an integer factor.

The coefficient decimation (CD) technique was originally proposed for the realization of reconfigurable filters [3] and frequency response masking (FRM) technique was proposed for low complexity sharp transition-band finite impulse response (FIR) filters [8]. Recently, a reconfigurable low complexity channel filter for channelization supporting multiple standards has been proposed in [9, 10]. The objective of the work in [9, 10] was to realize a channel filter to extract a single channel from the wideband input signal and hence more suitable for radio handsets than base stations. However, MWCRs involves extraction of multiple channels of various communication standards in base stations and hence reconfigurable FB is needed. A reconfigurable FB based on FRM approach is proposed in [11] which provides a low complexity solution for non-uniform channelization. The FB proposed in [11] designs separate bank of masking filters for each communication standards and hence has limited reconfigurability. The number of channels in FB proposed in [11] depends on the value of delay selected, and the channel BW is fixed for a given delay and modal filter.

In the proposed FB, fixed bank of masking filters is used independent of communication standard and value of delay is also fixed. The proposed FB is able to overcome the limitations of reconfigurability, non-uniform BW, fixed channel stacking mentioned earlier in this section. The proposed FB is compared with conventional PC approach, DFTFB, GFB and the MPRB for multiplier complexity.

The proposed FB, PC approach and DFTFB are implemented on Virtex FPGA and area, power and delay comparisons are presented.

2.2 Review of Coefficient Decimation Approach

The proposed FB is based on interpolation, CD [3] to obtain multi-band response and frequency masking technique to extract each band. In [3], two techniques namely coefficient decimation-1 (CD-I) and coefficient decimation-II (CD-II) are proposed for the realization of reconfigurable FIR filters.

In CD-I, every *Dth* coefficient of an FIR filter is kept unchanged and all other coefficients are replaced by zeros to get multiband response with identical passband width and transition-band width *(TBW)* as that of the original filter. By changing the value of D, different number of frequency response replicas located at integers multiples of $2\pi/D$ can be obtained [3]. Figure 1b, c shows the frequency response of filter obtained using CD-I from the modal filter in Fig. 1a. In the proposed FB, the CD-I approach is used for the design of masking filters and is explained in detail in Section 4.

In CD-II, every D^{th} coefficients of an FIR filter are grouped together discarding in between coefficients to obtain a decimated version of the original frequency response whose passband width and *TBW* are D times that of original filter [3]. Figure 1d shows the frequency response of filter obtained using CD-II from the modal filter in Fig. 1a. In CD-II, stopband attenuation (SA) reduces as D increases. Hence, original modal filter should be designed with larger SA taking into account of the deterioration caused by decimation. The CD-II approach is used to obtain variable BW frequency responses in this work and is explained later in Sections 3 and 4.

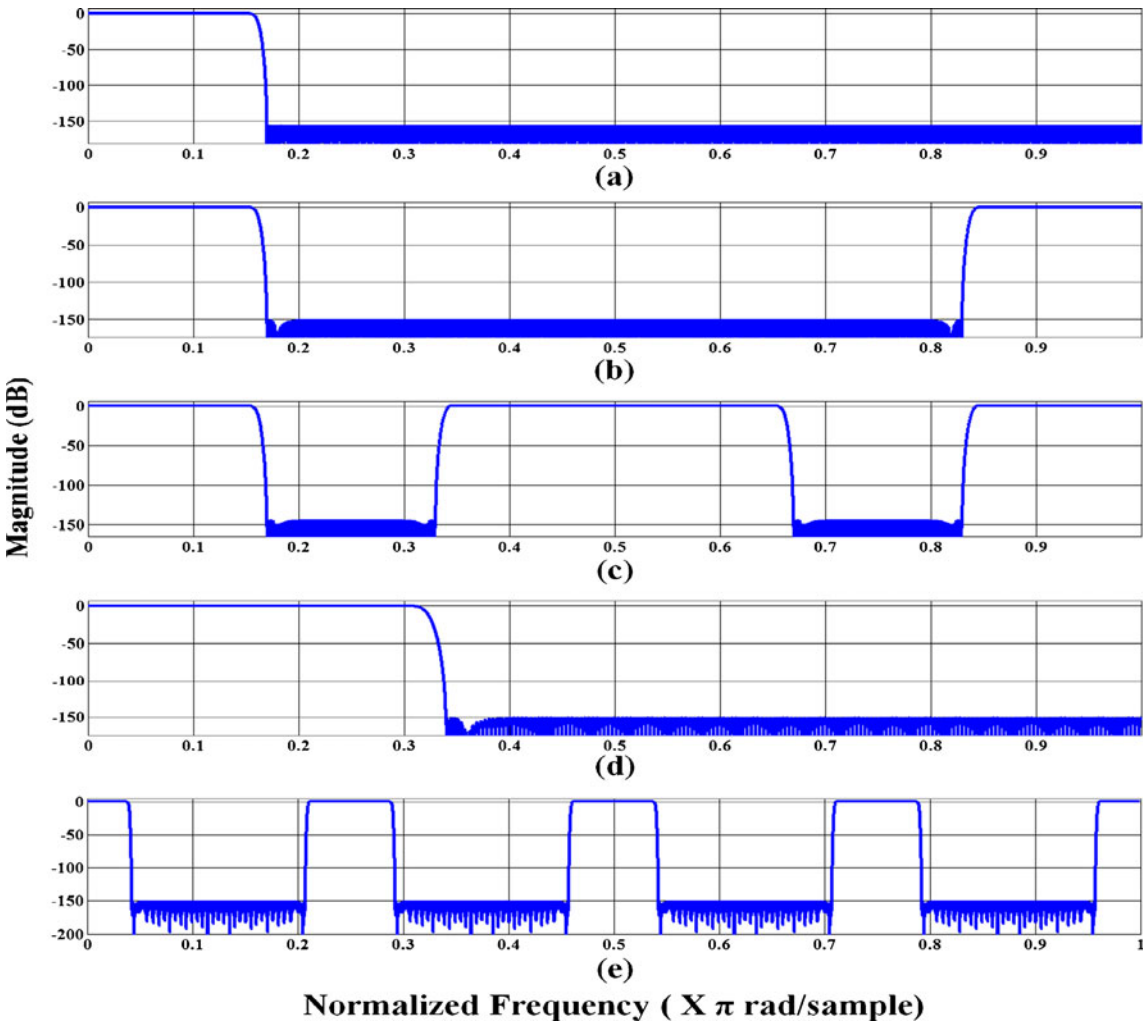

Figure 1 **a** Frequency response of modal filter, **b** Frequency response of filter using CD-I from modal filter in (**a**) for D=2, **c** Frequency response of filter using CD-I from modal filter in (**a**) for D=4, **d** Frequency response of filter using CD-II from modal filter in (**a**) for D=2, **e** Frequency response of filter using Interpolation from modal filter in (**a**) for M=8.

Interpolation by M consists of replacing each delay element of an FIR filter by M delay elements resulting in a filter with $(M+1)$ multiband responses having passband width and TBW of each subband M times smaller than the original filter [8]. Figure 1e shows the frequency response of filter obtained using interpolation from the modal filter in Fig. 1a. The interpolation approach is used to obtain $(M+1)$-band filter and is explained later in Section 3.

3 Proposed Filter Bank Design

In MWCRs, the FB specification varies depending on the communication standards in operation at a specific time. In the conventional multi-standard FB channelizer [12, 13], reconfigurability is achieved by switching among different FBs, each designed for a particular standard. But this approach leads to inefficient resource utilization and increased hardware complexity. In this paper, we present a method to realize reconfigurable FB which will allow receivers to extract multiple radio channels of different BWs from the received wideband signal. An introductory idea of using the proposed FB for uniform and non-uniform channelization in MWCRs is discussed in [14] and it is noted that parts of the material in this paper have been presented in the conference paper [14]. However, in this paper, the idea discussed in [14] has been extended by including the complete design details, actual implementation results on FPGA and comparison with other FBs.

The block diagram of the proposed FB is shown in Fig. 2. It consists of three stages: 1) A low pass linear phase FIR filter called the modal filter, $H_a(z^{M/D})$, with CD-II, interpolation and complementary filter, $H_c(z^{M/D})$, to obtain multiband response, 2) Banks of masking filters to extract desired channels of interest, and 3) Adder Block to combine the subbands obtained from the masking filter stage. The first stage of the FB provides distinct BW subbands. The number of subbands depends on interpolation factor, M while subbands BW and TBW depends on decimation factor, D and interpolation factor, M. The outputs of modal filter and complementary filter are fed to respective fixed masking FBs. Each masking filter will extract the desired channel for which the masking filter is designed, by masking the frequencies of other channels. The number of masking filters depends on number of subbands produced by first stage. However, using CD-I technique discussed in Section 2, 2 or more subbands can be extracted simultaneously using single masking filter. It is done by decimating the masking filter with two or more decimation factors and subtracting the appropriate outputs from each other. This helps in reducing complexity of the proposed FB. The detailed discussion about the design of masking filters is given in Section 4. Output of second stage is given to adder block which combines adjacent subbands, if necessary, to extract the desired channels of interest. The variable decimation factor, D and adder block makes the proposed FB suitable for uniform and non-uniform channelization. The detailed design of proposed FB is given below.

3.1 Design of Modal Filter

The first stage of the proposed FB architecture consists of a modal filter whose passband width can be changed using suitable decimation factor D employing CD-II. The resultant filter is interpolated by a factor of M resulting in an $(M+1)$-band filter response (i.e. $H_a(z^{M/D})$) as shown in Fig. 2, with a BW and TBW which is D/M times that of the BW and TBW of the modal filter frequency response [10]. Thus, the first stage provides variable BW subbands, whose design steps are as follows:

Step-1 Determine the minimum subband BW (B) and maximum TBW, $TBW_{filterbank(max)}$ of the FB taking into account of the specifications of multiple communication standards under consideration.

Step-2 The value of M decides the number of subbands in the FB and is fixed to a single value. The objective of the proposed FB is to obtain both uniform as well as non-uniform BW subbands. Depending

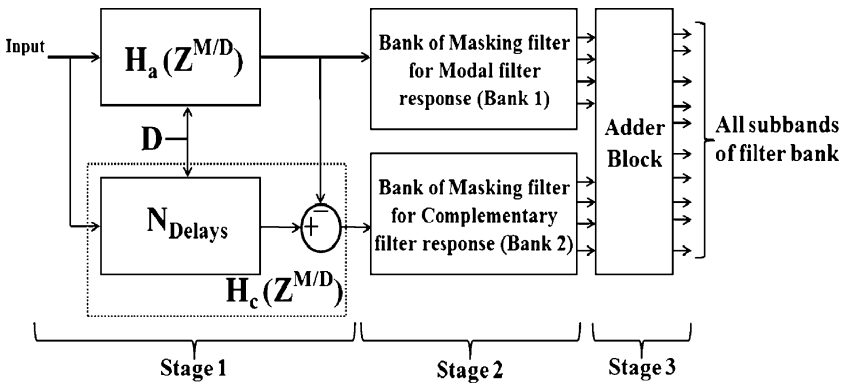

Figure 2 Block diagram of the proposed Filter Bank.

upon the value of M, uniform subband BW ($B_{uniform}= 1/M$) can be obtained.

Step-3 Consider the N-tap low pass filter (called modal filter) with passband and stopband edges as F_{pass} and F_{stop} respectively. All the frequency edges mentioned in this paper are frequencies normalized with respect to sampling frequency. Let the D takes integer values from D_{min} to D_{max}. As discussed later in this Section, when $D=D_{min}$, all the subbands in modal filter response have minimum BW, B and when $D= D_{max}$, all the subbands in complementary filter response have minimum BW, B. Hence, mathematically we can write,

$$\frac{F_{pass} \times D_{\min}}{M} = \frac{B}{2} \tag{1}$$

$$\frac{F_{pass} \times D_{\max}}{M} = \frac{1}{M} - \frac{B}{2} - TBW_{filterbank(\max)} \tag{2}$$

Step-4 When all the subbands are of uniform bandwidth (i.e. $B=1/M$) and $D=D_{uniform}$, then we can write

$$F_{pass} \times D_{uniform} = 0.5 \tag{3}$$

From Eqs. (1), (2) and (3), we can obtain appropriate values of F_{pass}, D_{min}, D_{max}. The frequency response of the N-tap modal filter should be well within the normalized Nyquist frequency i.e. $F_{stop} \leq 1/D_{\max}$ [3].

Step-5 In the modal filter design, stopband attenuation is decided by D_{max}, which corresponds to the most stringent specification, i.e., highest order filter taking into account of the frequency response deterioration for D_{max}. If the required SA of the FB is $\partial_{s(filter\ bank)}$, then the SA of modal filter is given as $(\partial_{s(filter\ bank)}/D_{\max})$ [10]. Generate an N-tap modal filter with passband and stopband edges as F_{pass} and F_{stop} respectively and stopband attenuation of $(\partial_{s(filter\ bank)}/D_{\max})$.

Step-6 Complementary filter response is obtained by subtracting modal filter response from appropriate delayed version of the input signal. Due to CD-II by factor D and interpolation by factor M, effective length of modal filter is increased by M/D. Number of delays to obtain complementary response is given as,

$$N_{delays} = \left\{ \left(\left\lfloor \frac{(N-1)}{D} \right\rfloor + \left(\left\lfloor \frac{(N-1)}{D} \right\rfloor \bmod 2 \right) \right) \times \frac{M}{2} \right\} \tag{4}$$

The design process in steps (1–4) is shown in Fig. 3. In Fig. 3, H_a represents the modal filter response and H_c represents the complementary filter response. Figure 3a shows the frequency response of modal filter ($H_a(z)$) and complementary filter ($H_c(z)$). In Fig. 3b, the frequency response of decimated and interpolated modal filter response ($H_a(z^{M/D})$) and its complementary ($H_c(z^{M/D})$) when $D=D_{min}$ is shown, where D_{min} is the minimum value of D. Figure 3c shows the frequency response of decimated and interpolated modal filter response ($H_a(z^{M/D})$) and its complementary ($H_c(z^{M/D})$) when $D=D_{max}$, where D_{max} is the maximum value of D. Figure 3b and c show how channel BW can be varied by changing D.

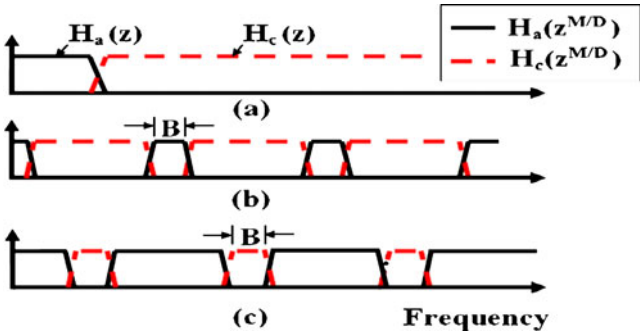

Figure 3 Frequency response showing the design of modal filter.

3.2 Design of Masking Filter

The second stage of the proposed FB consists of lower order masking filters designed to extract variable BW subbands obtained from the output of first stage. Figure 4a shows the variation of subband BW of modal filter ($H_a(z^{M/D})$) as D is varied. Similarly, Fig. 4b shows the variation of subband BW of complementary filter ($H_c(z^{M/D})$) as D is varied. As the value of D is increased from D_{min} to D_{max}, BW of the subbands in modal filter response increases and BW of subbands in complementary filter response decreases.

The proposed FB consists of two banks of masking filters 1) for modal filter response (*Bank 1*), and 2) for complementary filter response (*Bank 2*) as shown in Fig. 2. The two masking FBs, *Bank 1* and *Bank 2* are designed independently. The same masking filters can be used to

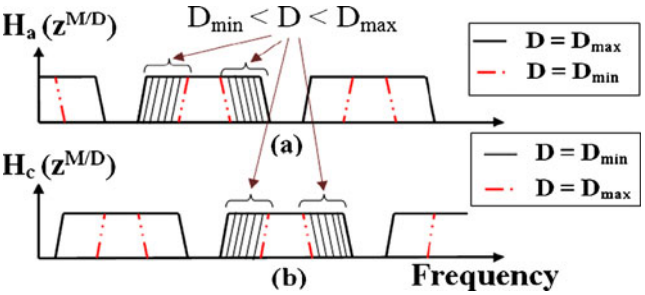

Figure 4 Frequency response of the modal filter and complementary filter for different values of D.

separate the distinct BW channels obtained using different decimation factors. Hence, there is no need to reconfigure the masking filters; instead fixed coefficient masking filters can be employed. Implementation complexity of fixed-coefficient filters can be reduced by realizing multiplication operation using shift and add operation [15, 16] and incorporating the multiplier block technique to reduce the number of adders [17]. The passband and stopband frequencies of masking filters of *Bank 1* are obtained using the frequency plot of $H_a(z^{M/D})$ for $D=D_{max}$ shown in Fig. 5. Similarly, the passband and stopband frequencies of masking filters of *Bank 2* can be obtained using frequency plot of $H_c(z^{M/D})$ for $D=D_{min}$. The design equations for masking filters (as can be observed from Fig. 5) are specified below:

1. The passband frequencies of masking filter ($F_{p(mask)}$) are given as,

$$\begin{aligned} F_{p1(mask)} &= F_{centre\,1} - TBW_{filterbank(\max)} + B/2 \\ F_{p2(mask)} &= F_{centre2} + TBW_{filterbank(\max)} - B/2 \end{aligned} \tag{5}$$

2. Similarly, stopband frequencies of masking filter ($F_{s(mask)}$) are given as,

$$\begin{aligned} F_{s1(mask)} &= F_{centre\,1} + TBW_{filterbank(\max)} - B/2 \\ F_{s2(mask)} &= F_{centre\,2} - TBW_{filterbank(\max)} + B/2 \end{aligned} \tag{6}$$

where B is the minimum channel BW, ($F_{centre1}$,$F_{centre2}$) are the centre frequencies of adjacent bands in the complementary response as shown in Fig. 5 and $TBW_{filterbank(max)}$ is the maximum TBW of each subband when $D=D_{max}$. Note that interpolation factor, M is fixed. When M is changed, the number of subbands and their centre frequencies changes. Hence, different set of masking filters are required when M is changed.

For *(M+ 1)*-channel FB, conventional approach [11, 18] is to use one masking filter with passband and stopband frequencies given by Eqs.(5) and (6) for each channel. Though this approach reduces design effort significantly, it leads to increase in hardware complexity and power consumption. It is not necessary to design separate masking filter for each channel. The number of masking filters can be reduced significantly by employing the CD-I approach, which is explained in more details in Section 4.

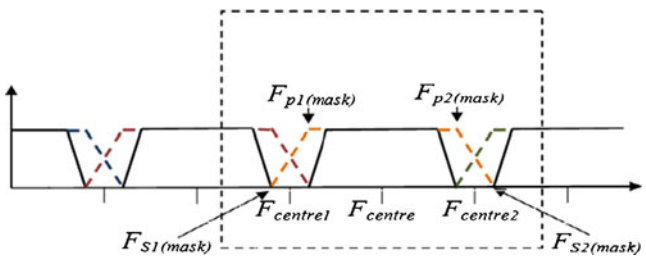

Figure 5 Frequency plot indicating the passband and stopband frequencies of masking filter when $D=D_{max}$.

3.3 Design of Adder Block

The third stage of the proposed FB consists of adder block. The main purpose of adder block is to achieve the problem of non-uniform BW channel extraction and overcome the fixed channel stacking. The adder block is designed such that all the combinations of additions of up to 4 adjacent bands are obtained. The detailed design of adder block is explained in Section 4.

4 Filter Bank Architecture

In this section, we present the reconfigurable architecture of the proposed FB. A model based design using Matlab Simulink and Xilinx System generator was employed for the implementation purpose as shown in Fig. 6 (copied directly from the Simulink environment). It shows three blocks : Lyrtech signal master controller [19], input signal and Xilinx hardware co simulation (hwcosim) block along with the simulink representation of the architecture.

The Lyrtech signal master controller consists of three components, (1) the board configuration for configuring the FPGA/DSP and for downloading the bit-stream to FPGA, (2) Xilinx's system generator for generating the bit stream to be downloaded to the FPGA, and (3) Log viewer which gives implementation information about the area and delay of the architecture used. The input signal block provides the real time input for the proposed architecture. We have generated the bitstream of the simulation architecture using the Xilinx system generator. The generated bitstream can be downloaded to FPGA and it appears as a 'Lyrtech Cosim Engine' block as shown in Fig. 6. The performances of the bitstream and the simulation architecture were checked to ensure that they are identical.

For illustrative purpose, we have chosen B=0.06 and M= *8* so that a 9-channel FB is obtained. The F_{pass} and F_{stop} of modal filter are selected as 0.083 and 0.115 respectively. The decimation factor D is varied from 3 to 7. Taking into account the maximum deterioration due to D_{max} which is 7 in this case, the SA of FB is taken as −40 dB. The length of the modal filter obtained using Bellanger's formula [20] is 276. For D=6, all the 9 channels are of uniform BW (identical to that of the DFTFB).

The sub-blocks of the proposed FB are shown in Fig. 7 representing the inputs and outputs of the three stages of the proposed FB. The detailed architecture of each sub-block is shown in Figs. 8, 9, 10 and 11. Next, the design of each sub-block of the proposed FB is discussed in detail.

The first stage consists of modal filter with CD-II and interpolation and complementary delays to get complementary response. The detailed architecture of the modal filter

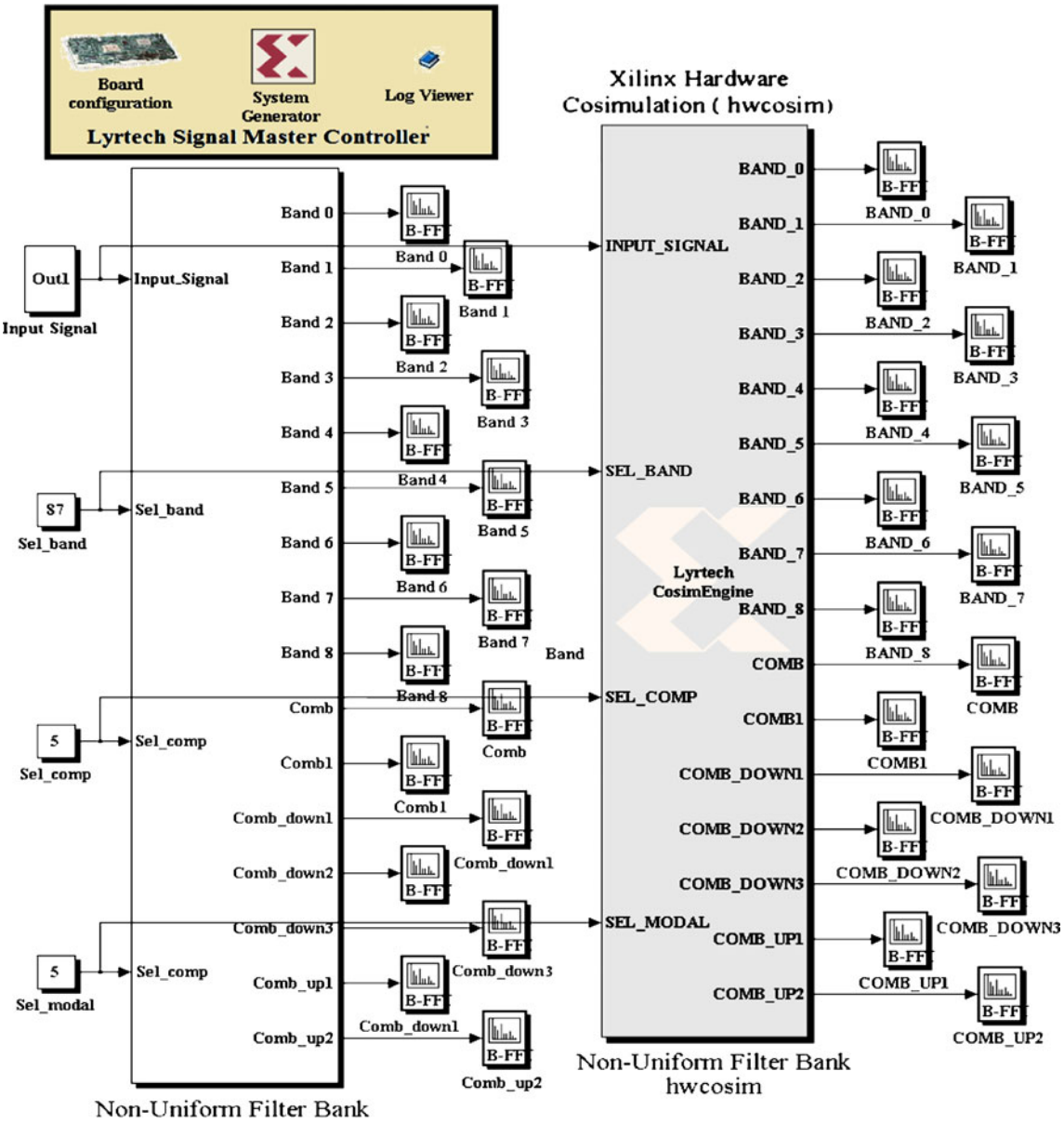

Figure 6 Implementation of the proposed FB architecture on Virtex 2v3000ff1152-4 FPGA.

is shown in Fig. 8. All the filters in the proposed FB are implemented with transposed direct form structure so that the critical path delay is independent of the filter length. Here, each delay in the filter is replaced by 8 delays which means interpolation by factor 8. The inputs to modal filter are input signal, mux control signals Sel_modal and Sel_comp. The suitable value of D is obtained using these mux control signals. Both the signals Sel_modal and Sel_comp are 5 bit wide i.e. 1 bit for each D. For example, 00001, 00010 indicates that D is 3 and 4 respectively and so on. When *Sel* input for mux is '0', mux passes the *D0* input and for *Sel* value '1', mux passes the *D1* input. For D=3, filter coefficients 1,4,7,10... are selected and for D=6, filter coefficients 1,7,13.. are selected. Here, *OR* gate is used which selects filter coefficient 7 in both cases. Upper part of Fig. 8 gives modal filter response and output of lower part is subtracted from an appropriate delayed version of input signal to get complementary filter response. The control signal Sel_comp is used to select appropriate delayed version of input depending on the value of D. Figure 12 shows the frequency response of the modal filter obtained by varying D from 3 to 7 for F_{pass}=0.083, F_{stop}=0.115. It can be observed that very fine control over subband BW is possible in the proposed FB.

Both the outputs of modal filter and complementary filter are passed to the second stage which consist of banks of masking filters as shown in Fig. 7. The masking filters are used to extract all channels obtained from first stage and

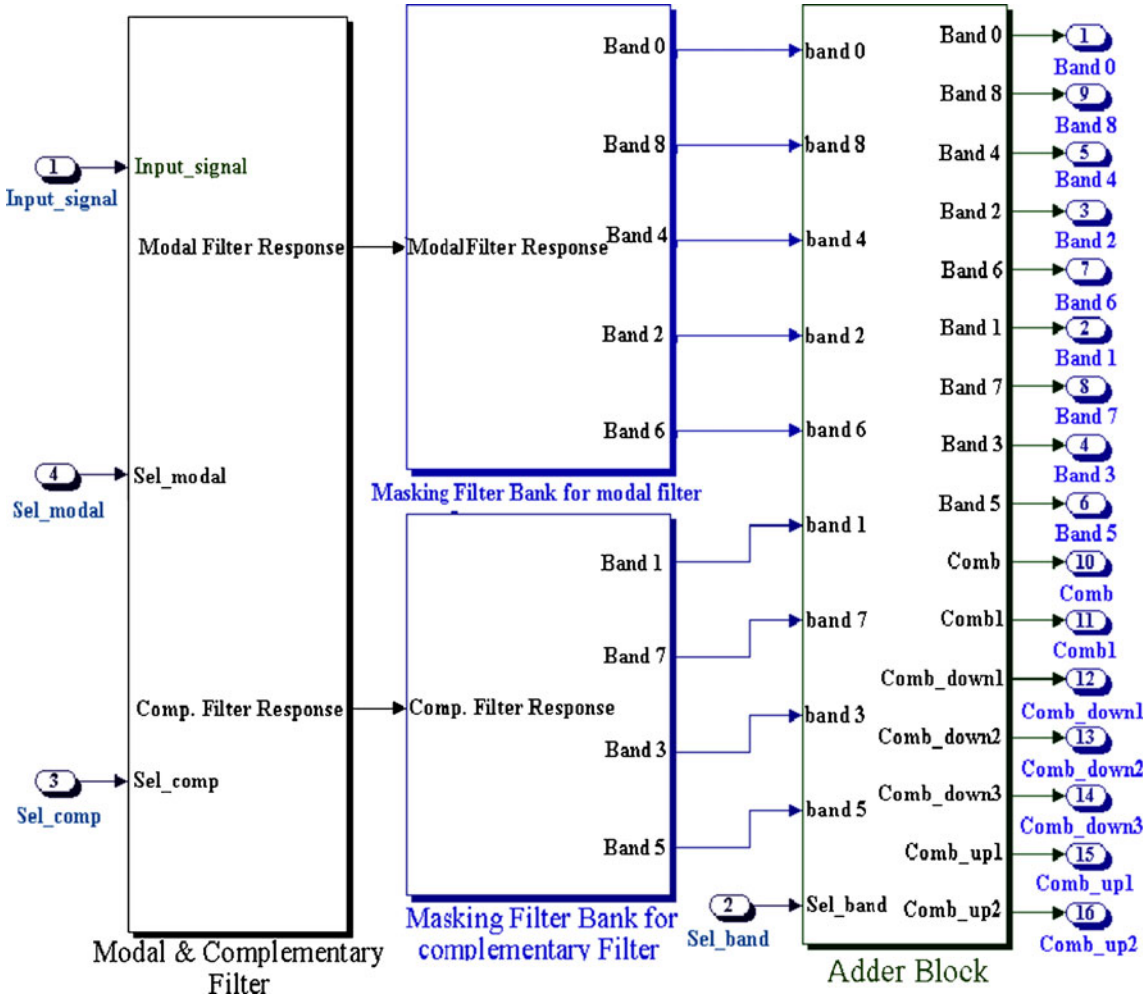

Figure 7 Three stages of FB 1) Modal and complementary filter, 2) Masking filter, 3) Adder block.

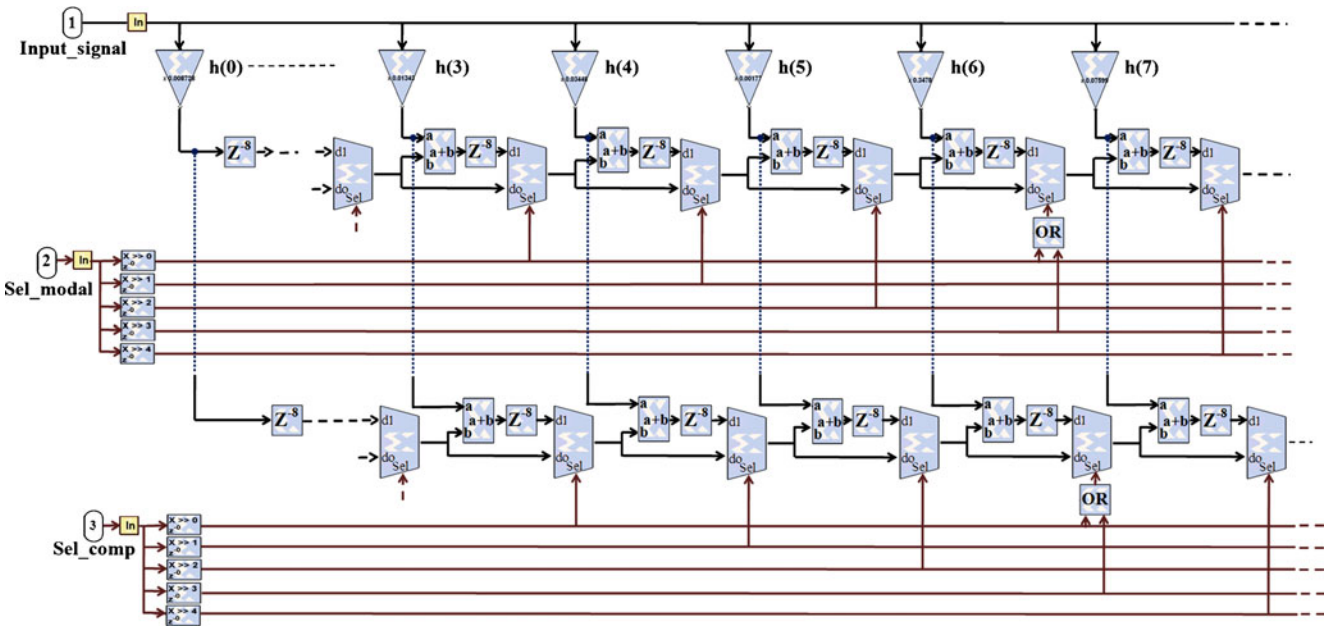

Figure 8 Architecture of modal filter.

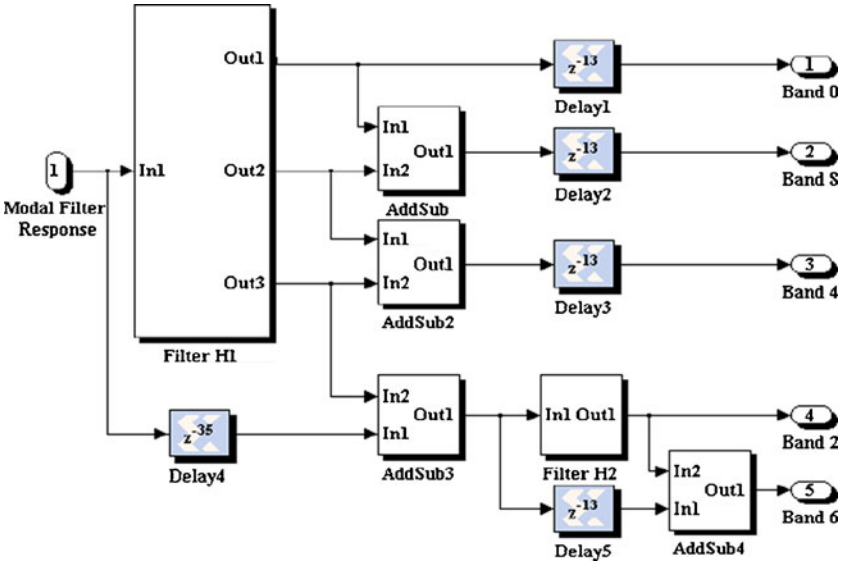

Figure 9 Architecture of Bank1 of masking filter.

are designed using Eqs. (5) and (6). Using conventional masking techniques [11, 18], 9 masking filters are required to separate 9 bands (*band-0* to *band-8*) shown in Fig. 12. However, advantages of CD-I can be used to reduce the number of masking filters from 9 to 4. The architecture of second stage of proposed FB consisting of banks of masking filter, shown in Figs. 9 and 10. First masking filter $H_1(z)$ is designed to extract *band-0*. Then, using CD-I with value of D as 2 on $H_1(z)$, we get *band-0* and *band-8* together (according to Fig. 1b) and by subtracting *band-0*, we get *band-8*. Similarly using CD-I with value of D as 4 on $H_1(z)$, we get *band-0*, *band-4, band-8* together according to Fig. 1c and by subtracting *band-0* and *band-8*, we get *band-4*. Thus, using a single masking filter, and CD-I, three bands can be extracted. Finally, *band-2* and *band-6* can be extracted by using single lower order low pass masking filter $H_2(z)$ and its CD-I with D=2.

The bandpass masking filter $H_3(z)$ is used to extract *band-3* in complementary response and its CD-I with D=2 is used to get *band-5*. Finally, *band-1* and *band-7* can be extracted by using lower order masking filter $H_4(z)$ and its CD-I with D=2. Thus, the use of CD technique in the proposed FB helps in reducing the number of masking filters providing computationally efficient architecture. The extracted subbands are delayed by an appropriate delay value before passing to third stage. The value of delay depends on the order of masking filters and is selected such that group delay of all extracted subbands at the input of second stage (i.e. adder block) is same.

The adder block architecture shown in Fig. 11 combines the adjacent subbands in order to obtain channels of wider BWs. The number of subbands that can be combined are limited to four to reduce the complexity. The adder block consist of two stages. The inputs to this block are the subbands (i.e. *band-0—band-8*) extracted from second stage (i.e. masking filter stage) of the proposed FB and mux control signal Sel_band. The signal Sel_band is 6 bit wide and can be used to extract any subband of interest. In the first stage of adder block, non-adjacent subbands (such as *band-0* and *band-8* or *band-1* and *band-7* and so on) are given to the

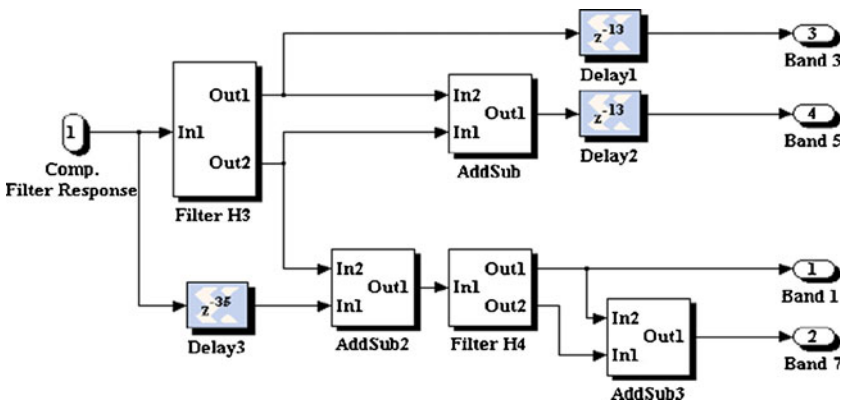

Figure 10 Architecture of Bank2 of masking filter.

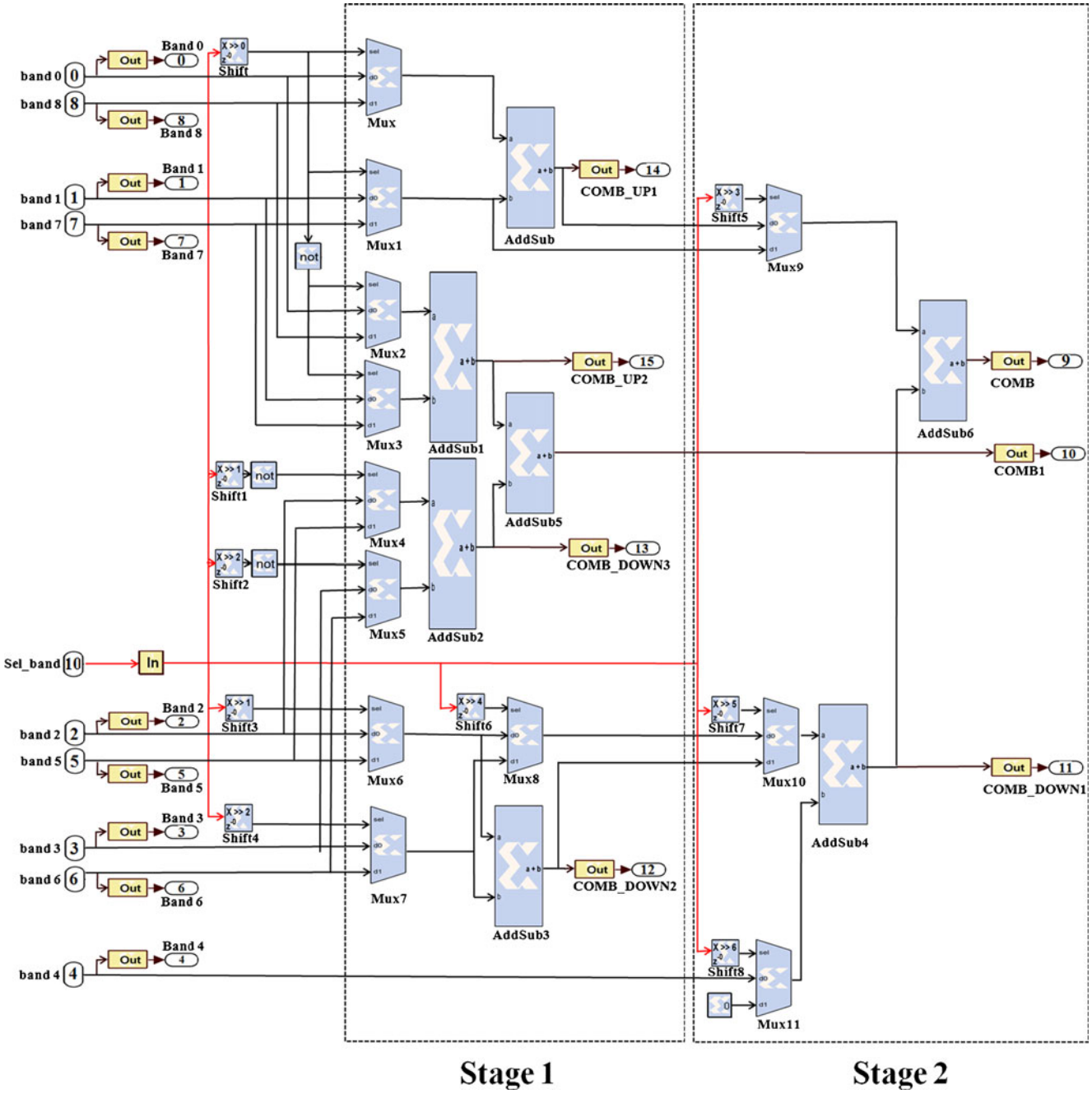

Figure 11 Architecture of Adder Block.

2-input multiplexers. This is because we do not require *band-0*, *band-8* together as a output in practical situation. Output of multiplexers are combined to obtain outputs COMB_UP1, COMB_UP2, COMB_DOWN2, COMB_-DOWN3 as shown in Fig. 11. For example, output COMB_UP1 consists of either *band-0* and *band-1* together or *band-7* and *band-8* together depending on the value of Sel_band. Second output COMB_UP2 is complementary to COMB_UP1 such that when the output COMB_UP1 consists of addition of *band-0* and *band-1*, COMB_UP2 consists of addition of *band-7* and *band-8* and vice versa. Similarly, outputs COMB_DOWN2, COMB_DOWN3 contain addition of either *band-2* and *band-3* or *band- 5* and *band-6*.

In the second stage of adder block, output of first stage are given to 2-input multiplexer. The outputs of multiplexers are combined to obtain COMB_DOWN1, COMB and COMB1. Table 1 shows the band obtained for some of the combinations of Sel_band. It is also possible to combine more than 4 subbands but at the cost of increases adder and multiplexer complexity. Thus, at the output of third stage of proposed FB, we get original subbands extracted by second stage along with the non-uniform subbands obtained from

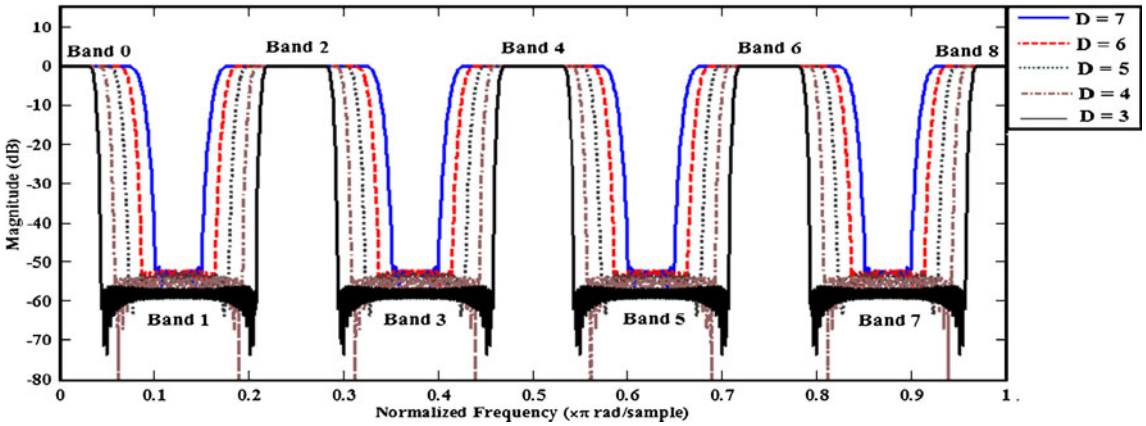

Figure 12 Channel BW variation for modal filter with F_{pass}=0.083 and F_{stop}=0.115, for different decimation (D) factors.

combinations of adjacent subbands making the proposed FB architecture suitable for non-uniform channelization.

From the above discussion, we note that, in the proposed FB, the BW of subbands can be varied by changing the decimation factor D and/or by suitably chosen Sel_band signal. The proposed architecture offers reconfigurability at two levels, filter level and architectural level.

4.1 Filter Level Reconfigurability

In the proposed FB, reconfigurability is achieved by suitably changing the decimation values for a fixed interpolation value to extract channels of different BW. Theoretically, we can extract $(M+1).(D_{max}-D_{min}+1)$ number of channels of distinct BWs. In the above design example, the decimation factor is varied from 3 to 7 by selecting appropriate Sel_modal, Sel_comp and a fixed value of M (=8) is used. Thus, $9.(7-3+1)=45$ channels of distinct BWs shown in Fig. 12 can be extracted using only 4 fixed coefficient masking filters. The specifications of all the channels corresponding to D=3 to 7 for modal filter with F_{pass}=0.083, F_{stop}=0.115 are listed in Table 2. It is clear from Table 2 that passband width of *band-0* can be varied from 0.0311 to 0.0726 by changing D as illustrated in Fig. 8.

Another level of reconfigurability can be exploited by reconfiguring the coefficients of the modal filter to change its F_{pass} and F_{stop}. However, there is limitation on minimum and maximum values of F_{pass} and F_{stop} of modal filter such that BW of channels is not less than B and hence, same masking filters can be used. From Fig. 3, it is clear that we get channels of BW B when D is D_{min} or D_{max}. Hence, the maximum passband frequency of modal filter ($F_{pass(max)}$) for $(M+1)$–channel FB is given by,

$$F_{pass(\max)}=\left\{\left(\frac{1}{M}-\frac{B}{2}\right)\times\frac{M}{D_{\max}}\right\} \tag{7}$$

Minimum passband frequency of modal filter ($F_{pass(min)}$) for $(M+1)$–channel FB is given by,

$$F_{pass(\min)}=\left\{\frac{M\times B}{D_{\min}\times 2}\right\} \tag{8}$$

The maximum and minimum stop band frequencies ($F_{stop(min)}$, $F_{stop(max)}$) of modal filter are obtained by adding TBW of modal filter to corresponding passband frequencies such that $\{F_{stop(\max)}\times D_{\max}<1\}$ to avoid aliasing. Coefficients of modal filter can be stored in LUT. As discussed in Section 2, no. of coefficients in modal filter are less compared to the convention filter implementation due to CD-II and interpolation. Therefore, size of LUT is small. One more advantage of the proposed FB is that only 4 fixed coefficient masking filters are needed to extract all $K.(M+1).(D_{max}-D_{min}+1)$ channels corresponding to K modal filters with $F_{stop(min)}\le F_{stop}\le F_{stop(max)}$, $F_{pass(min)}\le F_{pass}\le F_{pass(max)}$. For K=2, we can extract 90 channels of distinct BWs. The specifications of all the channels corresponding to D=3 to 7 for modal filter with F_{pass}=

Table 1 Specification of channels extracted by adder block for different values of sel_band.

Sel_band	COMB	COMB1	COMB_UP1	COMB_UP2	COMB_DOWN1	COMB_DOWN2	COMB_DOWN3
1000000	0+1+2	5+6+7+8	0+1	7+8	2	2+3	5+6
0100000	0+1+2+3+4	5+6+7+8	0+1	7+8	2+3+4	2+3	5+6
0111111	4+5+6+7	0+1+2+3	7+8	0+1	4+5+6	5+6	2+3
0101000	1+2+4	5+6+7+8	0+1	7+8	2+3	2+3	5+6

Table 2 Specification of passband and stopband frequencies of channels for different modal filters.

Band no.	D	Modal filter specifications							
		F_{pass}=0.083 and F_{stop}=0.115				F_{pass}=0.067 and F_{stop}=0.1			
		F_{stop1}	F_{pass1}	F_{pass1}	F_{stop2}	F_{stop1}	F_{pass1}	F_{pass1}	F_{stop2}
1	3			0.0311	0.0431			0.0251	0.0375
	7			0.0726	0.1			0.0586	0.0875
2	3	0.0311	0.0431	0.2069	0.2189	0.0251	0.0375	0.2125	0.2249
	7	0.0726	0.1	0.15	0.1774	0.0586	0.0875	0.1625	0.1914
3	3	0.2069	0.2189	0.2811	0.2931	0.2125	0.2249	0.2751	0.2875
	7	0.15	0.1774	0.3226	0.35	0.1625	0.1914	0.3086	0.3375
4	3	0.2811	0.2931	0.4569	0.4689	0.2751	0.2875	0.4625	0.4749
	7	0.3226	0.35	0.4	0.4274	0.3086	0.3375	0.4125	0.4414
5	3	0.4569	0.4689	0.5311	0.5431	0.4625	0.4749	0.5251	0.5375
	7	0.4	0.4274	0.5726	0.6	0.4125	0.4414	0.5586	0.5875
6	3	0.5311	0.5431	0.7069	0.7189	0.5251	0.5875	0.7125	0.7249
	7	0.5726	0.6	0.65	0.6774	0.5586	0.5875	0.6625	0.6914
7	3	0.7069	0.7189	0.7811	0.7931	0.7125	0.7249	0.7751	0.7875
	7	0.65	0.6774	0.8226	0.85	0.6625	0.6914	0.8086	0.8275
8	3	0.7811	0.7931	0.9569	0.9689	0.7751	0.7875	0.9625	0.9749
	7	0.8226	0.85	0.9	0.9274	0.8086	0.8275	0.9625	0.9749
9	3	0.9569	0.9689			0.9625	0.9749		
	7	0.9	0.9274			0.9125	0.9414		

0.083, F_{stop}=0.115 and F_{pass}=0.067, F_{stop}=0.1 are listed in Table 2. Table 2 shows that passband width of *Band-0* can be varied from 0.0251 to 0.0726 by changing D from 3 to 7 using filter level reconfigurability. If PC approach were employed for channelization, separate filter for each of 90 channels would be required.

4.2 Architecture Level Reconfigurability

The reconfigurability of the proposed FB at architecture level enables the extraction of extremely narrowband signals from wideband input signal. This can be achieved by using different values of D for modal filter and complementary filter. For example, if we select Sel_modal as 00001 and Sel_comp as 10000, we can have modal filter response with D=3 and complementary filter response with D=7. In this case, passband width of *Band-0, Band-2, Band-4, Band-6* and *Band-8* is 0.06 and that of *Band-1, Band-3*, *Band-5* and *Band-7* is 0.05 for modal filter with F_{pass}=0.083, F_{stop}=0.115, M=8 and note that all subbands are narrowbands. But, as the decimation factor D is different for modal and complementary filters, adjacent subbands cannot be combined using adder block (i.e. third stage of the proposed FB) and hence, only *band-0* to *band-8* are the valid outputs of the adder block. Conventional channelizer based on the PC approach, DFTFBs and its modifications would require very higher order prototype filter to meet narrowband requirements.

When decimation factor D for *modal* and complementary filter is same, then adjacent subbands of FB can be combined using adder stage as discussed earlier. Thus, by employing reconfigurabilities at architectural and filter levels, the proposed FB can extract channels with non-uniform BW which is not possible in GFB, DFTFBs and its modifications. Also, the problem of fixed channel stacking and reformulation of DFT in DFTFB does not exist in the proposed FB. Furthermore, the proposed FB is able to receive channels of multiple standards simultaneously, where as separate filter banks would be required for simultaneous reception of multi-standard channels in a DFTFB based receiver.

5 Functionality Test

The functionality of our architecture for the different spectrum scenario is tested as follows. A wideband input signal as shown in Figs. 13a, 14a, 15a and 16a are given to the proposed FB. In each case, wideband input signal consists of channels of distinct BW. The BWs of different channels are given in Table 3. All the channels are successfully extracted using the proposed FB architecture by selecting appropriate value of Sel_modal, Sel_comp and Sel_band. For example, all the channels shown in Fig. 13a are extracted by choosing Sel_modal=1, Sel_comp=1 and Sel_band=34. The individual extracted channels are shown in Fig. 13b–f. Similarly, individual

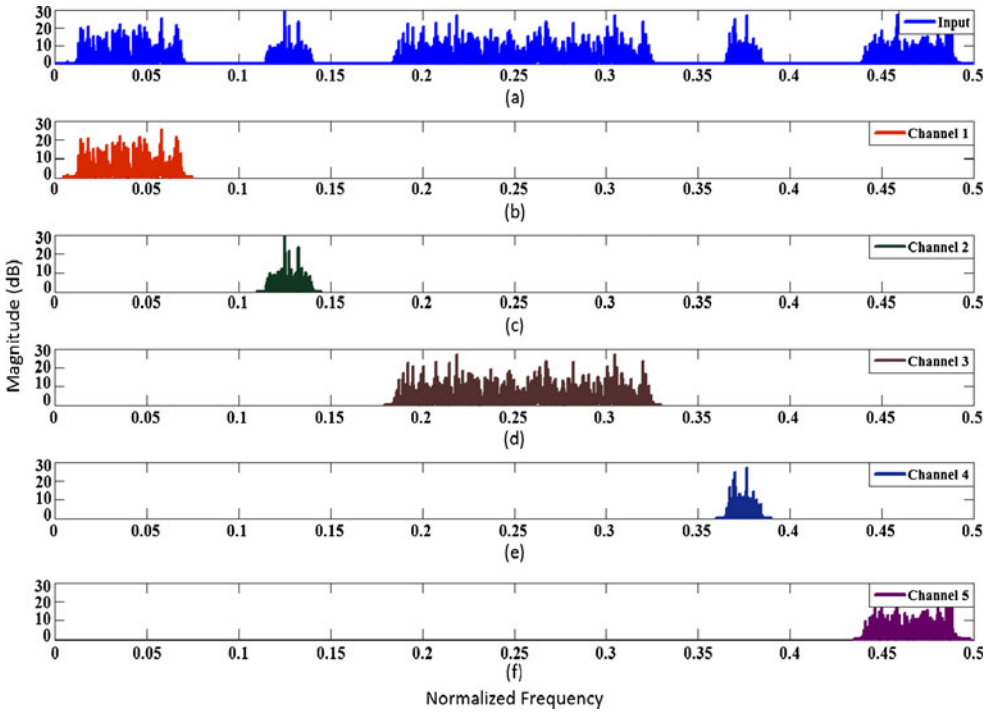

Figure 13 **a** Input signal consisting of 5 channels, **b–f** Extracted channels 1–5 using proposed FB.

extracted channels corresponding to input shown in Figs. 14a, 15a and 16a are shown in Figs. 14b–e, 15b–e and 16b–d respectively. Other FB architecture such as DFTFB, GFB and MPRFB need to reconfigure their prototype filter to extract channels corresponding to different inputs. Also, DFTFB and GFB cannot extract non-uniform channels. Though PC approach can be used for this application, it needs separate filters for each distinct channel in each input making the architecture highly complex and power consuming compared to the proposed FB.

To ensure that the proposed FB does not cause amplitude distortion, we calculate mean square error (MSE) using the formula,

$$MSE = \mathrm{E}\left\{(S_{ec} - S_{in})^2\right\} \tag{9}$$

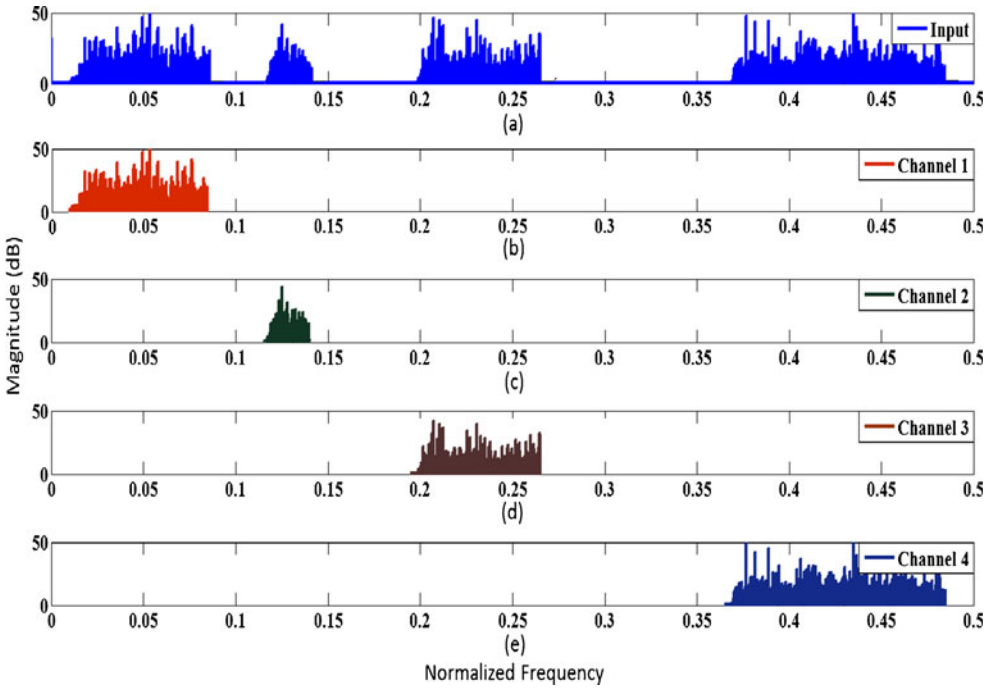

Figure 14 **a** Input signal consisting of 6 channels, **b–g** Extracted channels 1–5 using proposed FB.

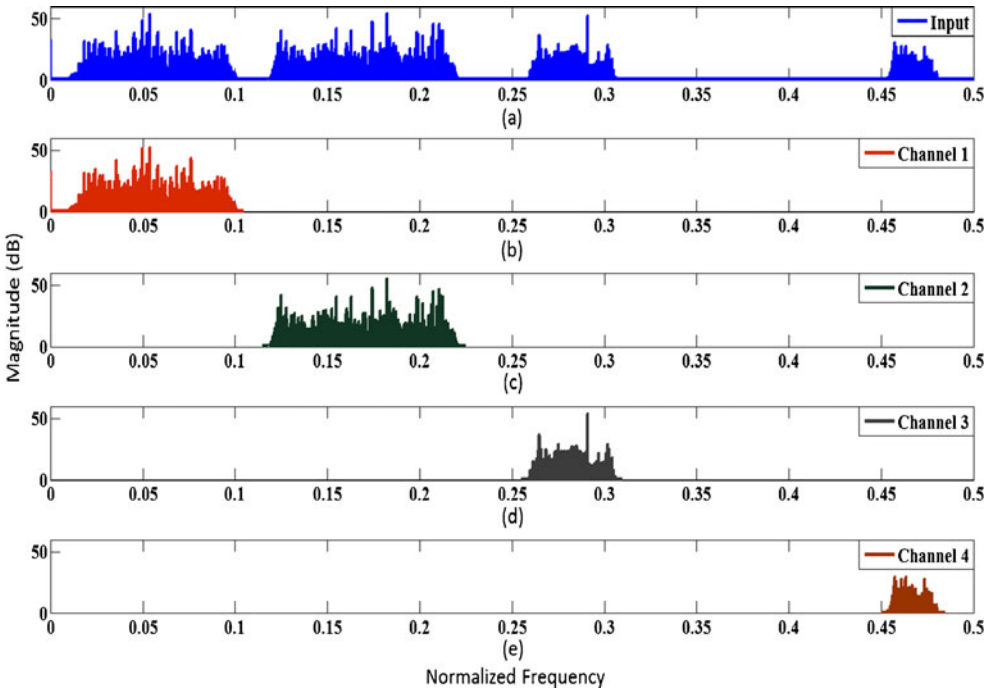

Figure 15 **a** Input signal consisting of 4 channels, **b**–**f** Extracted channels 1–4 using proposed FB.

where E is expectation operator, S_{ec} are the samples of extracted channels and S_{in} are the corresponding samples of input channel. The MSE should be as small as possible. MSE values for the results shown in Figs. 13, 14, 15 and 16 are given in Table 4. Note that the errors are low and NA denotes not applicable, as spectrum in Figs. 14, 15 and 16 have less than five channels.

6 Multiplication Complexity

Since multiplication is the most complex and power consuming operation in a digital FB, comparison of the proposed FB with other FBs in literature in terms of number of real-valued multiplication is presented in this section. As the proposed FB can produce uniform as well as

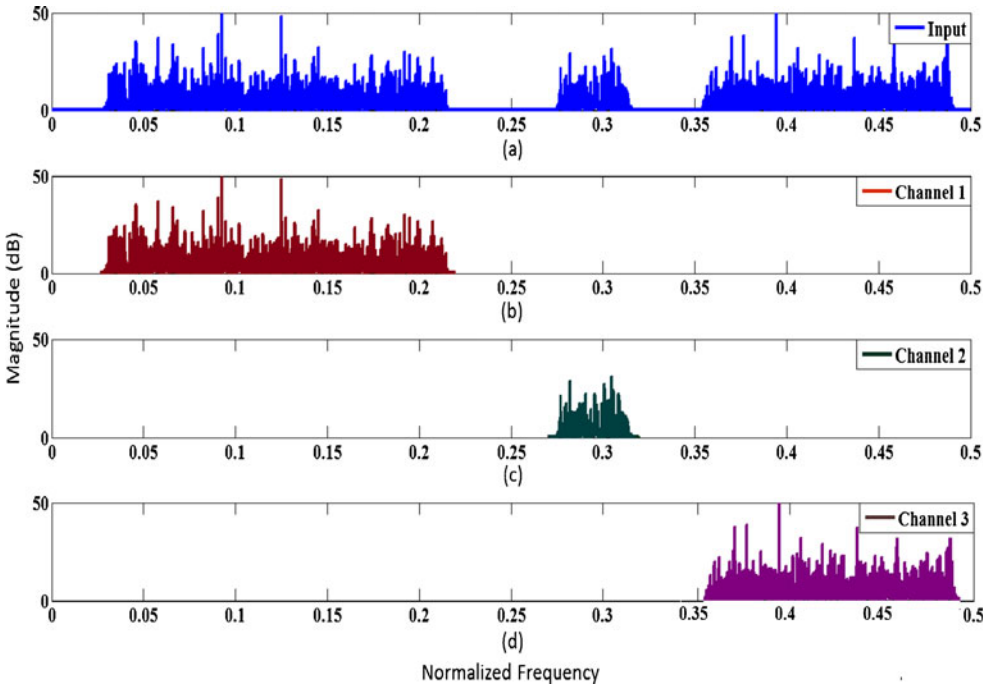

Figure 16 **a** Input signal consisting of 3 channels, **b**–**d** Extracted channels 1–5 using proposed FB.

Table 3 BW of different channels.

Channels	Channel BW (Fig. 13)	Channel BW (Fig. 14)	Channel BW (Fig. 15)	Channel BW (Fig. 16)
Channel 1	0.069	0.0797	0.09	0.185
Channel 2	0.033	0.02	0.1	0.041
Channel 3	0.15	0.04	0.05	0.134
Channel 4	0.03	0.12	0.02	NA
Channel 5	0.062	NA	NA	NA

non-uniform FB response, it is fair to compare the proposed FB as a uniform FB with uniform FBs—GFB and DFTFB and the proposed FB as a non-uniform FB with PC and MPRFB as a non-uniform FBs. In specific design example of the proposed FB presented in Section 3, filter length of modal filter is 276. Similarly, length of each masking filters $H_1(z)$, $H_3(z)$ is 65 and that of $H_2(z)$, $H_4(z)$ is 21 using Bellanger's formula [20]. As modal filter and all masking filters have symmetrical coefficients and transposed direct form filter structure is employed, number of multiplications is $\lceil N/2 \rceil$, where N is the filter length. Thus, the number of multiplications in our design example is 139 for modal filter, 33 each for $H_1(z)$, $H_3(z)$ and 11 each for $H_2(z)$, $H_4(z)$. Also, CD-II (which keeps every Dth coefficient and discards every other coefficients) is employed in modal filter and as D varies from 3 to 7, 48 out of 139 filter coefficients are discarded irrespective of any value of D from 3 to 7. Hence, total number of real multiplications is $91 + 33 + 33 + 11 + 11 = 179$.

For a fair comparison, 9 filters employed in PC approach are designed with same magnitude response specifications as that obtained by proposed FB with F_{pass}=0.083, F_{stop}= 0.115 and D=3 given in Table 2. The total number of real multiplications for the PC approach is 1080 (9 filters corresponding to 9 subbands each of length 240 with symmetric coefficients). Thus, our architecture consumes considerably less area, which is proportional to the reduction of number of multiplications, when compared to PC architecture. Moreover, in the proposed FB, bandwidth

Table 4 MSE for different channels.

Channels	MSE for spectrum Fig. 13.	MSE for spectrum Fig. 14.	MSE for spectrum Fig. 15.	MSE for spectrum Fig. 16.
Channel 1	0.1014	0.1004	0.1054	0.1090
Channel 2	0.0324	0.0366	0.0494	0.0992
Channel 3	0.0632	0.0197	0.0278	0.0623
Channel 4	0.0732	0.0992	0.0614	NA
Channel 5	0.0123	NA	NA	NA

Table 5 Number of multiplications for different fbs and comparison with proposed FB.

Channelization approach	No. of multiplications	% Saving of proposed FB
PC approach	1080	83.42
GFB	416	56.97
DFTFB	224	20.09
MPRB	448	60.04
Proposed FB	179	–

of subbands can be varied by changing D as discussed in Section 4. In PC approach, all the filters coefficients need to be updated to meet new specification which is time and area consuming.

The proposed FB divides spectrum from 0 to $F_s/2$ (where F_s is sampling frequency) into 9 channels. As mentioned in Section 4, the proposed FB produces output similar to 16-channel DFTFB and 16-channel MPRFB when D=6 with F_{pass}=0.083 and F_{stop}=0.115. For 16-channel DFTFB with −30 dB SA, total number of real multiplications is 224 (160 for prototype filter + 64 for DFT calculation). As complexity of MPRFB is double than that of DFTFB, total number of real multiplications is 448. Similarly, number of real multiplications in GFB is 416 (160 for prototype filter + 256 for modified Goertzel algorithm). Table 5 shows that the proposed FB offers complexity reduction of 83.42% over PC approach, 56.97% over GFB, 60.04% over MPRFB, 20.09% over DFTFB for D=6 case.

The number of real multiplications is a measure of the area complexity, and static power is directly proportional to area complexity. Thus, static power consumption of the proposed FB architecture is very less compared to PC approach, GFB, MPRFB, DFTFB. The dynamic power consumption of FB architecture depends on sampling rate at which filter is operated. The proposed FB operates at input sampling rate. The architecture based on PC approach, GFB, DFTFB and MPRB can be operated at lower sampling rate than input sampling rate due to polyphase decomposition [21]. Thus, dynamic power consumption of proposed FB is greater than other approaches. But, according to results in [22], static power consumption is more domination factor than dynamic power consumption

Table 6 Implementation results for proposed FB architecture.

Standard	PC approach	DFTFB	Proposed FB
Total slices	14334	11865	10157
Total power (mW)	1473	709	690
Total delay (nS)	11.533	26.549	30.12

for hardware implementation below 65 nm technology. In next Section, through synthesis results, we show that the overall power consumption of the proposed FB is less compares with other FBs.

7 Implementation Results

We have implemented the proposed FB, DFTFB, PC approach architecture on Xilinx Virtex 2v3000ff1152-4 FPGA associated with the dual DSP-FPGA Signalmaster kit provided by Lyrtech [19]. The Proposed FB is implemented with 16 bit precision while PC approach (design to extract channels corresponding to input shown in Fig. 14a) and 16-channel DFTFB are implemented with 14 bit precision. This is because number of taps (and hence number of slices and area) requirement in the proposed FB is low compared to other approaches. A model based design using Matlab's Simulink and Xilinx's System generator was employed for the implementation purpose. The system generator provides the hwcosim interface that makes it possible to directly incorporate a design running on signalmaster FPGA in a Simulink simulation. The bit stream of the proposed simulation architecture, generated using the Xilinx system generator, can be downloaded to FPGA using the board configuration block. The performance of the bit stream and the simulation architecture were checked to ensure that they are identical. The power consumption figures were calculated using X-power. The area results are obtained using log viewer block provided by Lyrtech. The implementation results are summarized in Table 6. Table 6 shows that the proposed FB offers area reduction of 29.14% over the PC approach and 14.39% over 16-channel DFTFB, static power reduction of 46.84% over the PC approach and 2.67% over 16-channel DFTFB. However, the total delay of the PC approach and that of the DFTFB are less than the total delay of the proposed FB by 38% and 12% respectively. Even though the proposed FB has a higher delay than the PC approach and DFTFB, the proposed FB is better choice for uniform and non-uniform channelization due to advantages of reconfigurability, variable subband BWs and area and power saving over the PC approach and DFTFB.

8 Conclusion

We have presented a new reconfigurable uniform and non-uniform FB architecture based on interpolation, CD and FRM for MWCRs. The proposed FB is capable of extracting channels of different BWs corresponding to multiple wireless communication standards from the digitized wideband input signal. We have functionally verified our architecture using real time Gaussian noise input. The proposed FB can extract non-uniform BW and very narrow BW channels compared to other FBs. Design example shows that the proposed FB offers complexity reduction of 83% over PC approach, 57% over GFB, 60% over MPRFB, 20% over DFTFB. Also, the proposed FB has an added advantage of dynamic reconfigurability over these FBs. The implementation results show that our method offers an average slice reduction of 29.14% over the PC approach designed for extracting all channels corresponding to the input shown in Fig. 14 with 14 bit precision and 14.39% over 16-channel DFTFB with 14 bit precision. The average reduction of power consumption achieved using our method over the PC approach is 46.84% and 2.67% over 16-channel DFTFB. However, the total delay of the PC approach and that of the DFTFB are less than the total delay of the proposed FB by 38% and 12% respectively.

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