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Guest Editorial: Special Issue on Embedded Signal Processing Circuits and Systems for Cognitive Radio-Based Wireless Communication Devices

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The demand for ubiquitous wireless services is ever-growing, and with the proliferation of mobile multimedia communication devices and wireless standards, it will continue to grow. Future communication devices have to support a plurality of applications such as text, speech, audio, video, and graphics. Apart from that, they also should be able to connect with many other devices operating on different standards. It has been observed that most of the licensed spectrum is largely underutilized, and similar views about the underutilization of the allocated spectrum have been reported by the Spectrum Policy Task Force appointed by the Federal Communications

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Commission (FCC). Motivated by this, new insights on cognitive radios have challenged the traditional static allocation approach to spectrum management. Cognitive Radio (CR), built on a Software-Defined Radio (SDR) platform is emerging as an environment-aware intelligent wireless communication system. It uses the methodology of understanding-by-building to learn from the environment and is able to adapt to statistical variations in the input stimuli, with the objective of achieving highly reliable communication at anytime and anywhere. This special issue brings together 10 papers that address various aspects of this challenge from the perspectives of wireless systems, computing architectures, embedded systems, and signal processing.

The original idea of SDR-based wireless communications is to digitize the signal directly after the antenna and replace the entire analog signal processing with digital signal processing. For a front-end with frequency range of 400 MHz (GSM) to 3.5 GHz (WiMax), the bandwidth of operation is about 3.1 GHz. The practical sampling rate of the signal is at least 2.5 times of the signal bandwidth resulting in about 7.7 Gsps in the present case. Such a high speed analog-to-digital converter (ADC) is very power intensive, and the data generated by the high speed ADC is required to be processed by a processor operating at similar or higher speed. The power consumption of processors operating at GHz clock frequency is also enormous. Thus the ideal SDR architecture is highly expensive and inefficient in terms of power and cost. This difficulty can be solved by the use of an RF front-end that can produce a desired band at IF band of relatively much lower width compared to the input bandwidth of the system. The first paper by Abhinav Kumar et al. presents an RF front-end architecture for wideband SDR. The authors present a partitioning mechanism that uses multiple medium bands to limit the intermodulation problem, which is a drawback of many existing wideband front-ends. This frequency partitioning scheme helps in achieving better performance along with relaxing the linearity requirement of devices.

An amplifier that can support multiple standards that are currently in use and those standards that may be introduced in the future is another requirement in SDR. Conventional multimode mobile equipments use several amplifiers connected in parallel to accommodate communication standards in frequency range 0.9–2.5 GHz. These amplifier architectures cause significant increase of the cost, size, and weight of mobile equipments. Furthermore, radios using amplifiers with predetermined frequency bands of operation cannot accommodate standards that may be introduced in the future. The second paper, by Nesimoglu, proposes frequency-tunable amplifiers to achieve the broad frequency coverage that is required for reconfigurable and multimode radios. This paper investigates the design of frequency-tunable amplifiers using various varactor diode topologies and the impact of tunable matching networks on power-added efficiency and linearity. Several tunable amplifiers using various varactor diode topologies as tunable devices are designed by using load-pull techniques, and their performances are compared in this work. It is shown that the amplifier using anti-series distortion-free varactor stack topology achieves 38% power-added efficiency, and it may be tuned from 1.74 to 2.36 GHz (about 35% tunable range). These amplifiers may facilitate the realization of frequency agile radio frequency transceiver front-ends and may replace several parallel connected amplifiers used in conventional multimode radios.

In the analog front-end of SDR, a down-conversion mixer often follows a low-noise amplifier (LNA). Due to the gain of the LNA, the mixer can have a higher noise

figure but also requires a higher input-referred third-order intercept point (IIP3). Because the input signal to the mixer is higher than that to the LNA, the linearity requirement of the mixer is more severe in comparison with the LNA. The third paper, by Amirabadi et al., presents a third-order intermodulation cancellation technique using nonlinear feedback as Pre-Post-Distortion for a low-power low-distortion mixer in deep sub-micron. This technique increases IIP3 and input 1 dB compression point to $+16.4$ dBm and -4.87 dBm, respectively. The mixer is designed in a 65-nm standard CMOS technology. Its layout indicates that the mixer occupies 0.315 mm $\times$ 0.296 mm of silicon area.

The concept of CR can be introduced to ultra-wideband (UWB) communications to minimize harmful interference and realize harmonic coexistence. Thus, a wideband RF front-end covering 3–10 GHz is very much desired from both CR and UWB point of view. In the fourth paper, Shi and Chia present the design of a 0.13-um CMOS noise-canceling wideband receiver front-end that achieves a 3-dB gain bandwidth of around 10 GHz spanning from 1.8 GHz up to 11.8 GHz. Comprising a wideband single-in-differential-out low-noise amplifier (LNA) and a quadrature double-balanced down-conversion mixer, the proposed design exploits noise cancellation in combination with inductive peaking techniques to extend the bandwidth and to lower the noise figure (NF) over the entire frequency band. A variable-gain method is developed for the LNA to switch between high-gain and low-gain modes as and when desired, without degrading the input impedance match. To obtain a robust design, parasitic effects of the chip package and electrostatic discharge protection devices are modeled and embedded in the RF front-end circuit. Together with a merged topology proposed for the quadrature mixer driven by a differential voltage buffer, this RF front-end achieves a very wide operating bandwidth with good gain and noise figure.

Direct conversion receivers in SDRs and CRs do not need high-Q bandpass channel select filters at high IF, and the channel select function is achieved by low-Q lowpass filters at baseband. Such receivers can be highly integrated and highly programmable since it is easier to integrate and reconfigure low-frequency lowpass filters than high-Q high-frequency bandpass filters. Therefore, the analogue baseband filter remains a critical performance-defining element in the design of integrated multistandard wireless transceivers. In the fifth paper, by Yichuang Sun et al., design considerations of tunable and programmable filters for highly-integrated multistandard receivers are presented. Circuit techniques for baseband filter design including the widely used active-RC and Gm-C circuits are described in this paper. Filter structures and design methods for higher-order baseband filters are reviewed, and on-chip tuning issues and methods are also discussed.

The high dynamic range and the large bandwidth of wireless communication signals set very strict requirements for the ADC in SDR and CR systems. One of the most promising radio architectures in this context is the low-IF or wideband direct-conversion multistandard receiver with a bandpass (BP) $\Sigma\Delta$ ADC. In the sixth paper, Jaakko Marttila et al. discuss the applicability of quadrature $\Sigma\Delta$ modulator (Q$\Sigma\Delta$M) based ADC in CR receivers. The authors propose a novel complex multiband Q $\Sigma\Delta$M scheme for the CR receivers. This multiband scheme allows parallel reception of scattered frequency chunks in the CR context and is stemming from the additional degrees of freedom in noise transfer function (NTF) design, provided by the Q $\Sigma\Delta$M principle.

This special issue continues with four papers that propose new digital signal processing architectures useful for SDR and CR. Parameterizing the hardware accelerators in the CR baseband incurs a latency penalty, which is a function of the amount of reconfiguration data required by the accelerator. In an opportunistic spectrum access scenario, the cumulative latency required to reconfigure all the physical layer units when switching to a new channel, reduces the useful time available for transmission leading to a lower system throughput. Against this background, the paper by Navin et al. gives an overview of the amount of reconfiguration data required by different candidate accelerator architectures for performing the computationally intensive channelization function in the digital front-end of the CR terminal. The paper also identifies opportunities for reusing hardwired stages of a channelization accelerator across multiple modes while minimizing the reconfiguration overhead.

The ability to accurately sense the presence of the rightful owners (primary users) is an important task of CR users (secondary users). Cooperative spectrum sensing emerges as an attractive alternative that exploits the inherent geospatial diversity of multiple cognitive radios to enhance the robustness of sensing accuracy. Two specific issues in cooperative spectrum sensing are discussed in the paper by Nguyen Duy Duong et al. The first issue is on dynamic detection of primary user's bands. A dynamic band clustering algorithm that uses K-means clustering technique is proposed in this paper. This algorithm reduces the number of erroneous narrow sub-bands resulting from spurious noise. This in turn minimizes the number of sub-bands to be detected and hence the overall sensing time. The second issue is on reducing the overheads required to facilitate fusion center operation. A novel entropy-based maximal ratio combining for decision-fusion center is also proposed in this paper.

In some CR applications, such as Dynamic Spectrum Access, the CR terminal should be able to modify its transmission parameters in order to communicate with efficient utilization of the spectrum resource. In such a case, the CR terminal would be capable of reconfiguring itself with minimum supplementary information to achieve the best performance. Against this background, Adel Metref et al. propose a blind carrier recovery loop with respect to the modulation scheme suited to CR applications in the paper titled "A carrier recovery loop for cognitive radio applications." Unlike conventional solutions which use a separate modulation identification device before performing carrier recovery, the proposed loop employs a hierarchical symbol decision to achieve phase lock, and then the S-curve and the variance of a decision-directed phase error detector are used to extract the information about the modulation scheme of the incoming signal. After the phase lock with the hierarchical decision, the constellation used in the received signal is detected, and then the true decisions are used to drive the recovery loop. Results obtained with different digital linear modulations indicate that the proposed loop is capable of achieving a real-time modulation scheme detection as well as keeping phase lock in case of adaptive modulation scheme transmissions.

System on chip implementation of high-performance Wireless Personal Area Networks (WPAN) is under development, and IEEE 802.15.3a standard is intended for the development of such a WPAN system with a target data rate up to 480 Mbps. Since it is targeted for a portable application, a low-power design is an implicit requirement. A Multiband OFDM-based physical layer (PHY) is the most popular

technology for IEEE 802.15.3a WPANs, and FFT/IFFT is one of the most computationally intensive components in such an OFDM-based PHY implementation, which approximately takes about 90% of the computational power of the baseband processor in the transmitter chain. Mathew et al. present an optimal implementation of 128-point FFT/IFFT for low-power IEEE 802.15.3a WPAN using pseudo-parallel datapath structure, where the 128-point FFT is devolved into 8-Pt and 16-Pt FFTs and then once again by devolving the 16-point FFT into 4×4 and 2×8. It is shown that the core power consumption with optimum case is 60.6 mW, which is less than half of the latest reported 128-point FFT design in 0.18-μ technology. Apart from the low power consumption, the advantages of the proposed architecture include reduced hardware complexity, regular dataflow, and simple counterbased control.

It is our hope that this special issue gives a wide coverage of the state-of-the-art in embedded signal processing circuits and systems for CR-based wireless communication technology and provides useful insights for further research in this area. We sincerely thank all the authors and the reviewers for their contributions.

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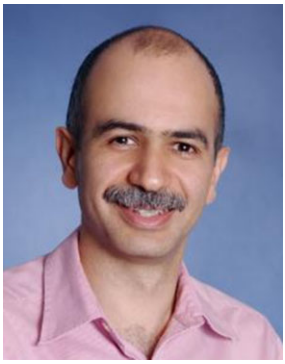

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